

Research article

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DESIGN OF GaAs pHEMT FRONT-END MMIC FOR DOWNCONVERTER

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Abstract. This paper details the design of a multifunctional front-end microwave monolithic integrated circuit (MMIC) intended for downconverter applications in the 1–3 GHz frequency range. The primary objective of this research is to develop a compact, high-performance MMIC that integrates three critical receiver functions – a low-noise amplifier (LNA), a 2-bit digital attenuator, and a single-pole five-throw (SP5T) switch – on a single gallium arsenide (GaAs) pHEMT die using a domestic technological process. The LNA employs a two-stage cascaded common-source configuration with RC-feedback networks to achieve wideband matching and low noise. The digital attenuator is constructed using a bridged T-network for 6 dB attenuation and a Π -network for 12 dB attenuation. The SP5T switch utilizes a series-shunt topology with a five-way combining junction to minimize chip area. Electromagnetic simulation results for the complete front-end demonstrate excellent performance, achieving a gain of no less than 29.9 dB, a noise figure not exceeding 1.21 dB, and an input and output return loss better than -8.4 dB across the operating band. The linearity figures, a P1dB of 20.6 dBm and an OIP3 of 30.1 dBm, confirm its suitability for demanding receiver systems. Furthermore, a comparative analysis against commercial analogues shows that the designed MMIC offers a competitive combination of wide bandwidth, low noise, moderate current consumption (under 85 mA at 5 V), and a compact layout (3.4×3.2 mm), validating its potential as a viable domestic alternative for high-performance microwave modules.

Keywords: GaAs pHEMT, MMIC, front-end, LNA, attenuator, SP5T

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РАЗРАБОТКА МОНОЛИТНОЙ ИНТЕГРАЛЬНОЙ СХЕМЫ ВХОДНОГО СВЧ ТРАКТА ДЛЯ ПРЕОБРАЗОВАТЕЛЯ ЧАСТОТЫ НА ОСНОВЕ GaAs pHEMT

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Аннотация. В данной работе подробно описывается разработка многофункциональной входной СВЧ монолитной интегральной схемы (МИС), предназначенной для применения в понижающих преобразователях частоты в диапазоне 1–3 ГГц. Основной целью исследования является создание компактной высокопроизводительной МИС, интегрирующей три ключевые функции приёмного тракта – малошумящий усилитель (МШУ), 2-битный цифровой аттенюатор и коммутатор на пять направлений с одним общим входом (SP5T) – на одном кристалле GaAs pHEMT, изготовленном на основе отечественного технологического процесса. МШУ построен по двухкаскадной схеме с общим истоком с цепями RC-обратной связи для обеспечения широкополосного согласования и низкого уровня шума. Цифровой аттенюатор выполнен на основе мостовой Т-образной схемы для ослабления 6 дБ и П-образной схемы для ослабления 12 дБ. Коммутатор SP5T использует последовательно-параллельную топологию с пятиплечевым объединяющим узлом для минимизации площади кристалла. Результаты электромагнитного моделирования полного входного тракта демонстрируют превосходные характеристики: коэффициент усиления не менее 29,9 дБ, коэффициент шума не более 1,21 дБ и потери на отражение по входу и выходу лучше –8,4 дБ во всей рабочей полосе. Показатели линейности – точка компрессии по уровню 1 дБ, равная 20,6 дБм, и точка пересечения третьего порядка OIP3, равная 30,1 дБм, – подтверждают пригодность схемы для применения в требовательных приемных системах. Кроме того, сравнительный анализ с коммерческими аналогами показывает, что разработанная МИС обеспечивает конкурентоспособное сочетание широкой полосы пропускания, низкого уровня шума, умеренного потребления тока (менее 85 мА при 5 В) и компактной топологии (3,4×3,2 мм), что подтверждает ее потенциал в качестве отечественной альтернативы для высокопроизводительных СВЧ-модулей.

Ключевые слова: GaAs pHEMT, СВЧ монолитная интегральная схема, входной тракт, малошумящий усилитель, аттенюатор, коммутатор

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW» (FSMR-2023-0008).

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Introduction

Modern radio engineering systems require the development of compact, highly efficient, and reliable building blocks, one of which is the frequency conversion module. A key trend in their design has been the use of microwave monolithic integrated circuits (MMICs) based on gallium arsenide (GaAs) pHEMT technology [1–3]. This technology provides an excellent combination of low noise, high gain, and good linearity in the microwave frequency range [4, 5].

Multifunctional MMICs, which integrate several devices on a single chip, are of particular practical interest. For example, an RF front-end (Fig. 1) comprising a low-noise amplifier (LNA), an attenuator, and a switch. The use of multifunctional MMICs enables significant reduction in module size, lower interconnection losses, improved repeatability of performance characteristics, and shortened design cycles – all of which underscore the relevance of this work [6–9].

Currently, the global semiconductor market faces a shortage of specialized solutions. Moreover, access to many foreign foundries producing GaAs-based MMICs is restricted. Therefore, particular emphasis is placed on expanding the range of MMICs manufactured using domestic technological processes (for instance, at JSC Svetlana-Rost) [10–12].

This paper examines the features of the design of a multifunctional front-end MMIC in the 1–3 GHz frequency range based on domestic GaAs pHEMT technology using integrated design tools for solid-state microwave devices (PDK_pHEMT05D).

The aim of this work is to design the topology of the front-end MMIC using domestic GaAs pHEMT technology, which integrates the functions of a LNA, a 2-bit attenuator, and a single-pole 5-throw (SP5T) switch.

The required specifications for the front-end MMIC are as follows:

- operating frequency range: 1–3 GHz;
- minimum gain: 25 dB;
- adjustable gain control within the range of 0–18 dB with a step of 6 dB;
- noise figure (NF) not exceeding 1.3;
- current consumption not exceeding 90 mA at a supply voltage of 5 V.

To achieve this aim, the following research tasks were formulated:

1. To conduct a comparative analysis of LNA, digital attenuator and switch to determine suitable structure of each subcircuit.

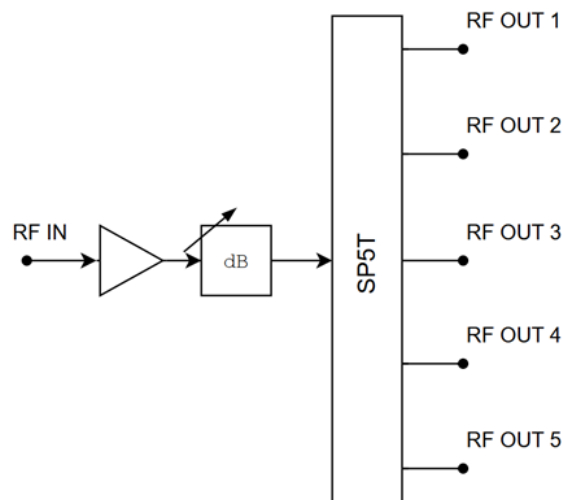


Fig. 1. Front-end block diagram

2. To calculate periphery of key elements (transistors, inductors, capacitors) to ensure the required specifications.

3. To evaluate the key electrical parameters (S-parameters, NF, P_{idB}) of whole front-end circuit through electromagnetic simulation and compare them with existing analogs.

LNA

LNAs are critical front-end components in any receiver system, responsible for amplifying weak signals received from the antenna while adding minimal noise.

The most fundamental challenge in LNA design is the inherent trade-off between noise and power matching. The minimum noise figure (NF_{min}) occurs at a specific source reflection coefficient Γ_{opt} , while maximum power transfer (minimum input return loss) requires the source impedance to be the complex conjugate of S_{11} ($\Gamma_s = S_{11}^*$). These two impedance points are generally different for a given transistor [13, 14].

The noise figure of a two-port can be expressed as:

$$NF = NF_{\text{min}} + \frac{4R_n}{Z_0} \cdot \frac{|\Gamma_s - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_s|^2) \cdot (|1 + \Gamma_{\text{opt}}|^2)}, \quad (1)$$

where R_n is the equivalent noise resistance and Z_0 is the characteristic impedance [15]. This equation shows that any deviation from Γ_{opt} increases the noise figure.

The most widely used technique to reconcile noise and input matching is source degeneration – a small inductor placed between the source terminal of the pHEMT and ground [13, 14, 16]. This inductive feedback has several beneficial effects:

1. It shifts Γ_{opt} toward the conjugate of S_{11}^* on the Smith chart, enabling simultaneous noise and power match.
2. It improves amplifier stability by increasing the Rollett stability factor [17]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}; \quad (2)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3)$$

and supplemental stability factor:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2. \quad (4)$$

3. It reduces the noise resistance R_n , making the noise figure less sensitive to impedance mismatch.

The most prevalent topology for GaAs pHEMT LNAs is the multi-stage cascaded common-source (CS) amplifier. This approach is used from S-band through Ka-band and beyond. RC-feedback topology is used for wideband matching. Since the feedback is negative, there is an accompanying decrease in gain with increasing feedback. Therefore, a compromise is generally made between the amount of improvement in VSWR/noise figure and the gain reduction one is willing to take [18].

The transistor gate width selection involves trade-offs between noise figure, gain, and power consumption. Smaller devices offer lower noise but also lower gain, while larger devices provide higher gain and better linearity at the cost of higher current consumption and noise [19].

Unconditional stability ($K > 1$ and $B1 > 0$ for all frequencies) is a mandatory requirement. Several stabilization techniques are employed:

- Source degeneration inherently improves stability [14].
- Series resistors at the drain output improve stability but reduce gain and increase noise, so they are typically used in later stages [15].

- RC networks (lossy match) are used in bias circuits to suppress low-frequency oscillations [18].

After comparative study of LNA, a stage-level design methodology is proposed:

1. **First stage:** optimized for minimum noise figure at the input, using source degeneration and noise-matched input network. Common approach for the first stage is to bias the transistor at approximately 10–30% of its saturation current (I_{dss}). Lower drain current generally yields lower NF_{min} but also lower gain, so a compromise must be found. The input matching networks must transform the $50\ \Omega$ source impedance to Γ_{opt} for minimum noise, while also providing reasonable return loss. Common techniques include:

- LC ladder networks;
- self-biased networks that simultaneously provide DC bias and RF matching;
- lossy match (resistive elements) to improve gain flatness at the expense of some increase in noise figure.

2. **Intermediate stages:** designed to provide maximum gain while maintaining flat frequency response. Interstage matching networks are carefully designed to maximize power transfer between stages while maintaining flat gain across the band.

3. **Final stage:** often uses a larger transistor and may be optimized for output power and linearity rather than noise.

The schematic of designed LNA is presented in Fig. 2. To achieve MMIC specifications two stages of CS transistors were used. Instead of using source degeneration and classic LC ladder networks, RC-feedbacks were implemented. This technique reduces number of inductors needed for transistor matching which leads to minimizing LNA topology.

It was calculated, that the best compromise between noise figure and gain is obtained when the first transistor has a periphery of $8 \times 45\ \mu\text{m}$ and is operated at 24.4 mA current, which is achieved with a drain-source voltage V_{d1} of 5 V and a gate-source voltage V_{g2} of $-1.1\ \text{V}$. At the next step, the bias networks (C2, C3, L2, R1, R3, R4), negative feedback network (C4, R2) were optimized for the best noise figure and highest associated gain.

The transistor dimensions of the second stage are taken higher than the first stage ($8 \times 80\ \mu\text{m}$ instead of $8 \times 45\ \mu\text{m}$) in order to improve the linearity of the amplifier. The bias conditions of the second stages

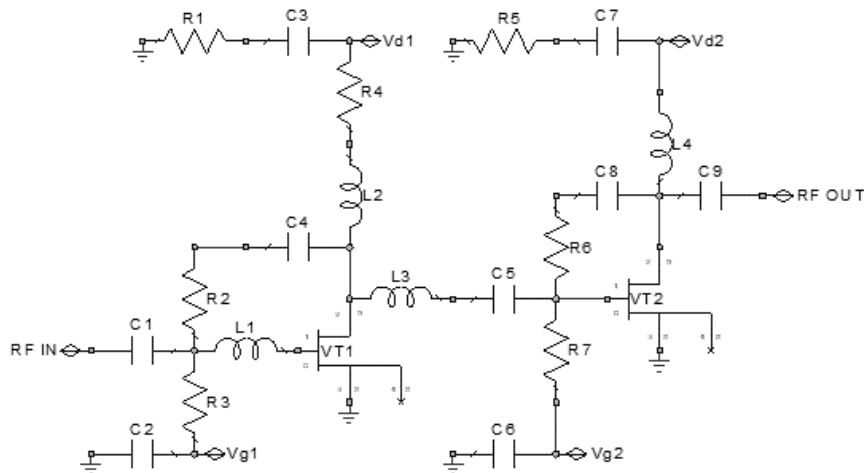


Fig. 2. Simplified schematic of LNA

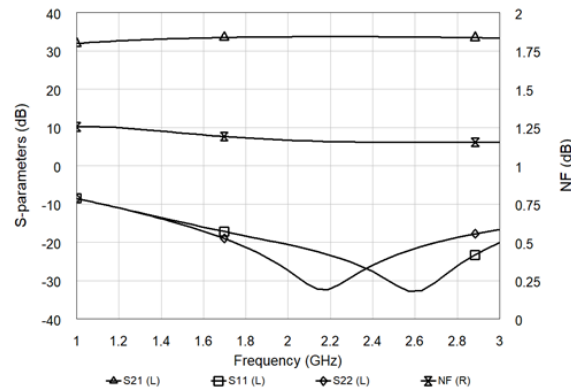


Fig. 3. S-parameters and NF of LNA

are identical ($V_{d2} = 5$ V and $V_{g2} = -1.1$ V, $I = 59.1$ mA). The bias networks (C6, C7, L4, R5, R7), negative feedback network (C8, R6) and interstage matching network (L3, C5) were optimized to achieve flat gain and highest linearity. Capacitors C1 and C9 are used for DC-blocking.

Simulation results of the designed LNA are presented in Fig. 3. Gain (S21) is no less than 31.8 dB, input and output return loss (S11 and S22) are less than -8 dB and NF does not exceed 1.26 dB.

The 1 dB compression point P_{1dB} of the LNA is 21.2 dB at 2GHz and the output third intercept point OIP3 for two close frequencies is 32.2 dB. Total current consumption is 83.5 mA at 5 V.

Digital attenuator

These devices provide precise, digitally controlled attenuation of RF signals with advantages over analog attenuators in terms of linearity, accuracy, thermal stability, and ease of control.

In digital attenuators, the GaAs pHEMT is operated in cold-FET mode (drain-source voltage is 0 V), where it functions as a voltage-variable resistor controlled by the gate voltage. When the gate voltage is 0 V, the channel is fully open and the drain-source resistance R_{on} is low (typically a few ohms). When the gate voltage is below the pinch-off voltage (e.g., -5 V), the channel is fully depleted and the device behaves as a small capacitor C_{off} in parallel with a large resistor.

The choice of pHEMT gate periphery (gate width W_g) involves a critical trade-off [20–23]:

- larger W_g leads to lower R_{on} , which means lower insertion loss and higher power handling;
- smaller W_g leads to lower C_{off} , which means better high-frequency isolation and broader bandwidth.

Digital attenuators are constructed by cascading individual attenuation bits, each providing a fixed binary-weighted attenuation value (e.g., 0.5, 1, 2, 4, 8, 16 dB). Different topologies are suited to different attenuation values and operating frequencies.

The switched T-type topology [20] consists of a series pHEMT switch (FET1), a shunt pHEMT switch (FET2), and two identical resistors (R1) in the series arms, plus a shunt resistor (R2) to ground. In the reference (low-loss) state, FET1 is ON and FET2 is OFF, providing a low-resistance path. In the attenuation state, FET1 is OFF and FET2 is ON, routing the signal through the resistive T-network to ground. This topology offers low insertion loss and good high-frequency capability because it uses a small number of devices with minimal parasitic capacitances. It is typically employed for small attenuation bits (1 and 2 dB).

For very small attenuation values (0.25, 0.5, and 1 dB), a simplified T-type topology omits the series switch transistor and one of the series resistors to reduce insertion loss [21, 22]. In this configuration, only a shunt pHEMT switch and a single resistor are used. When the shunt switch is OFF, the signal passes with minimal loss. When the shunt switch is ON, signal is partially shunted to ground through the resistor, creating the desired attenuation.

The bridged T configuration adds a series pHEMT switch across the two series resistors of the T-network, with a shunt switch connected to ground through a resistor [20, 22]. The bridged T offers a good trade-off between insertion loss, attenuation accuracy, and bandwidth. An appropriate series inductance can be added to create a resonant effect that improves isolation at high frequencies.

The Π -type attenuator uses a series pHEMT switch and two shunt pHEMT switches, along with three resistors [21–23]. Compared to the T-type, the Π -type can provide larger attenuation while maintaining good input/output return loss (VSWR), but occupies larger chip area at low microwave frequencies compared to T-type designs. It is therefore commonly used for medium-value bits such as 4 dB and 8 dB.

For the largest attenuation bits (typically 8 or 16 dB), the switched-path topology is often the preferred choice [22, 23]. This configuration uses two SPDT (Single-Pole Double-Throw) switches to select between a reference path (low-loss transmission line) and an attenuation path comprising a fixed resistive Π -network. This approach provides superior bandwidth and very low insertion phase shift between states, because the phase through the reference path can be compensated using a microstrip line of appropriate length.

Based on the reviewed literature, a design procedure for GaAs pHEMT digital attenuators can be summarized:

1. Select topologies per bit:
 - 0.25–1 dB: simplified T-type or switched T;
 - 2 dB: switched T or cascade of two 1 dB bits;
 - 4 dB: bridged T or Π -type;
 - 8 dB: Π -type or cascade of two 4 dB bits;
 - 16 dB: switched-path with SPDT switches or cascade of two 8 dB bits.
2. Calculate initial resistor values using standard formulas [24].
3. Select pHEMT sizes considering the trade-off between ON-resistance (insertion loss) and OFF-capacitance (bandwidth/isolation).
4. Place bits with better return loss at the input and output of the cascade to improve overall VSWR.
5. Perform EM simulation of the passive network (including all interconnect parasitics and via holes), optimize transmission-line dimensions and resistor values.

The functional assembly of the designed attenuator includes two sections with nominal attenuation of 6 dB and 12 dB respectively. Bridged T-network for 6 dB attenuation (Fig. 4, *a*) and Π -network for 12 dB attenuation (Fig. 4, *b*) were chosen to achieve a good trade-off between insertion loss, VSWR and attenuation accuracy.

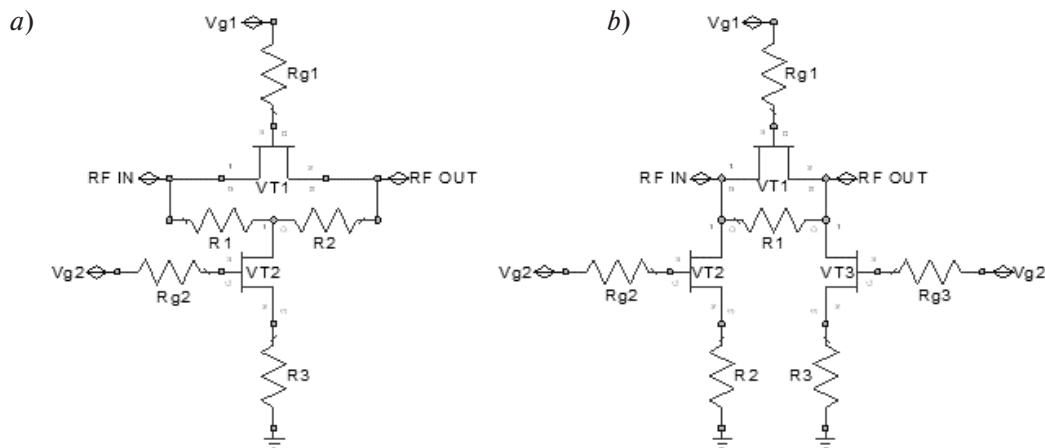


Fig. 4. Simplified circuits of attenuator sections: bridged T-network (*a*); Π -network (*b*)

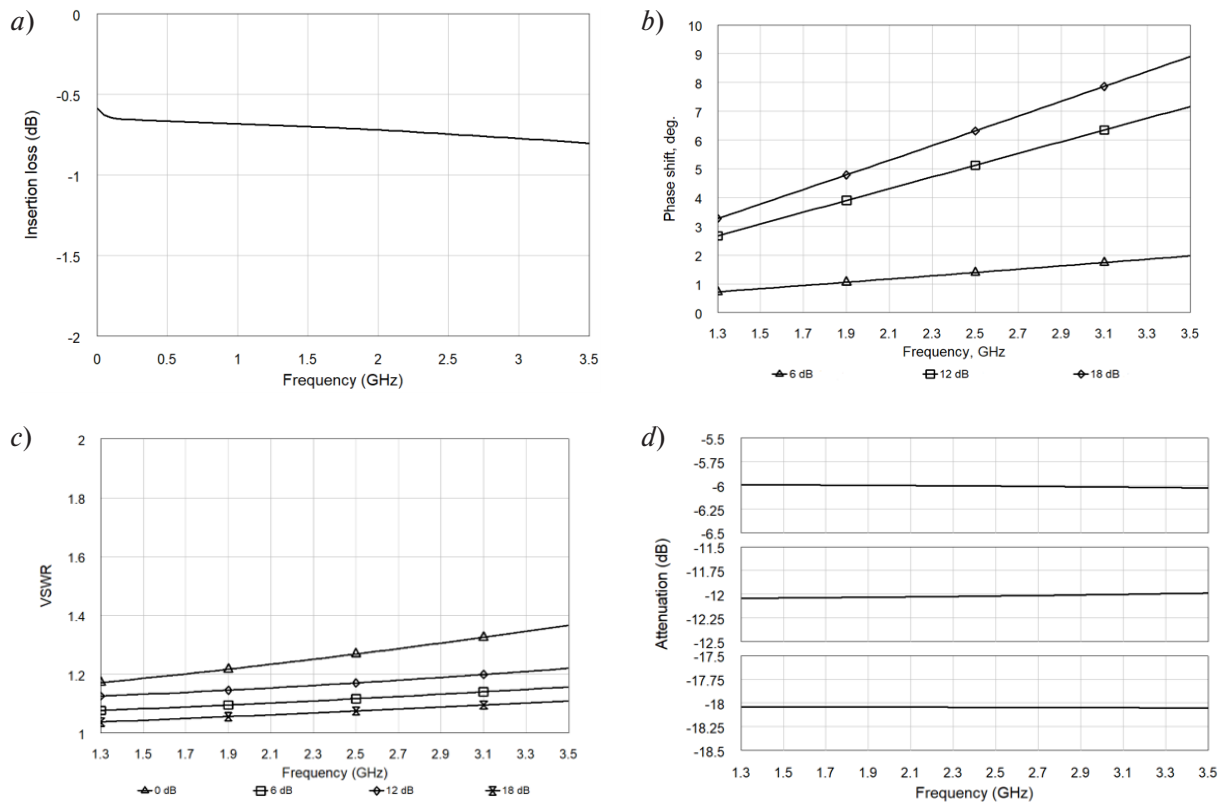


Fig. 5. Simulation results: insertion loss (a); phase shift (b); VSWR (c); attenuation (d)

Each section consists of switching FETs and metal film resistors. Element parameters obtained using parametric optimization are provided in Table 1. Large-valued gate resistors R_g (4.5 k Ω) are used to prevent RF leakage through bias lines while maintaining DC isolation.

Table 1

Element parameters

Element	T-network	Π -network
VT1	8×100 μm	8×50 μm
VT2	2×25 μm	2×30 μm
VT3	—	2×30 μm
R1	17.8 Ω	83.3 Ω
R2	17.8 Ω	16.7 Ω
R3	4 Ω	16.7 Ω

The results of the analysis of the attenuator are shown in Fig. 5. Insertion loss is less than 0.9 dB, VSWR is less than 1.4 and phase shift between reference state and attenuation states does not exceed 9 degrees.

SP5T switch

The design of such Single-Pole-Multi-Throw (SPMT) switches involves careful consideration of the circuit topology, device sizing, layout techniques, and matching networks to achieve low insertion loss, high isolation and good VSWR.

The FET gate periphery determines RF characteristics of a switch the same way as described for attenuators: large W_g decrease R_{on} (lower insertion loss) but increase C_{off} (lower isolation at high frequencies). Conversely, small W_g increase R_{on} (higher insertion loss) but decrease C_{off} (better isolation).

The choice of topology depends on the required number of throws, frequency band, and performance specifications.

The simplest switch topology uses a series-connected switch device in each branch. In SPDT form, when branch 1 is ON and branch 2 is OFF, the signal passes through the ON FET (low R_{on}) while the OFF FET presents a high impedance. However, at higher frequencies, the C_{off} of the shunt path provides a leakage path, degrading isolation [25].

In shunt-type switches, the FET is connected from the transmission line to ground. When the FET is ON, it creates a short circuit to ground, providing high isolation. When OFF, it presents a small capacitance that is resonated out by inductive elements or absorbed into the transmission line impedance [26, 27].

Combining series and shunt FETs in each branch yields the best trade-off between insertion loss and isolation. This topology is the most common for high-performance SPMT switches. The series FET provides the main signal path control, while the shunt FET to ground improves OFF-state isolation by providing a low-impedance path for leakage signals [28, 29].

For SPMT switches, the design challenges include:

- maintaining consistent channel-to-channel performance;
- managing layout parasitics due to increased routing complexity;
- ensuring impedance matching at the common junction.

Based on the reviewed literature, a design procedure for GaAs pHEMT SPMT switch is proposed:

1. Choose branch topology (series, shunt or series-shunt type);
2. Optimize pHEMT sizes considering the trade-off between insertion loss and bandwidth/isolation.
3. Match input and outputs for desired impedance.
4. Perform EM simulation of the passive network (including all interconnect parasitics and via holes).

The schematic of designed SP5T switch is presented in Fig. 6. Simulation showed that for 1–3 GHz frequency range series-shunt FET topology is the best choice for SPST branch. In order to reduce chip, the five-way combining junction is used instead of design SPDTs and directly connecting them to form SP5T switch. Each branch consists of $4 \times 60 \mu\text{m}$ series FET and $4 \times 80 \mu\text{m}$ shunt FET. Inductors

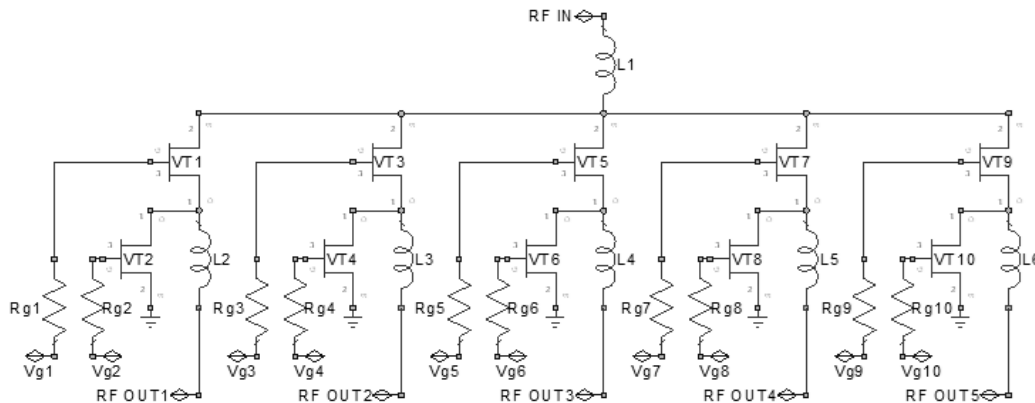


Fig. 6. Simplified schematic of SP5T switch

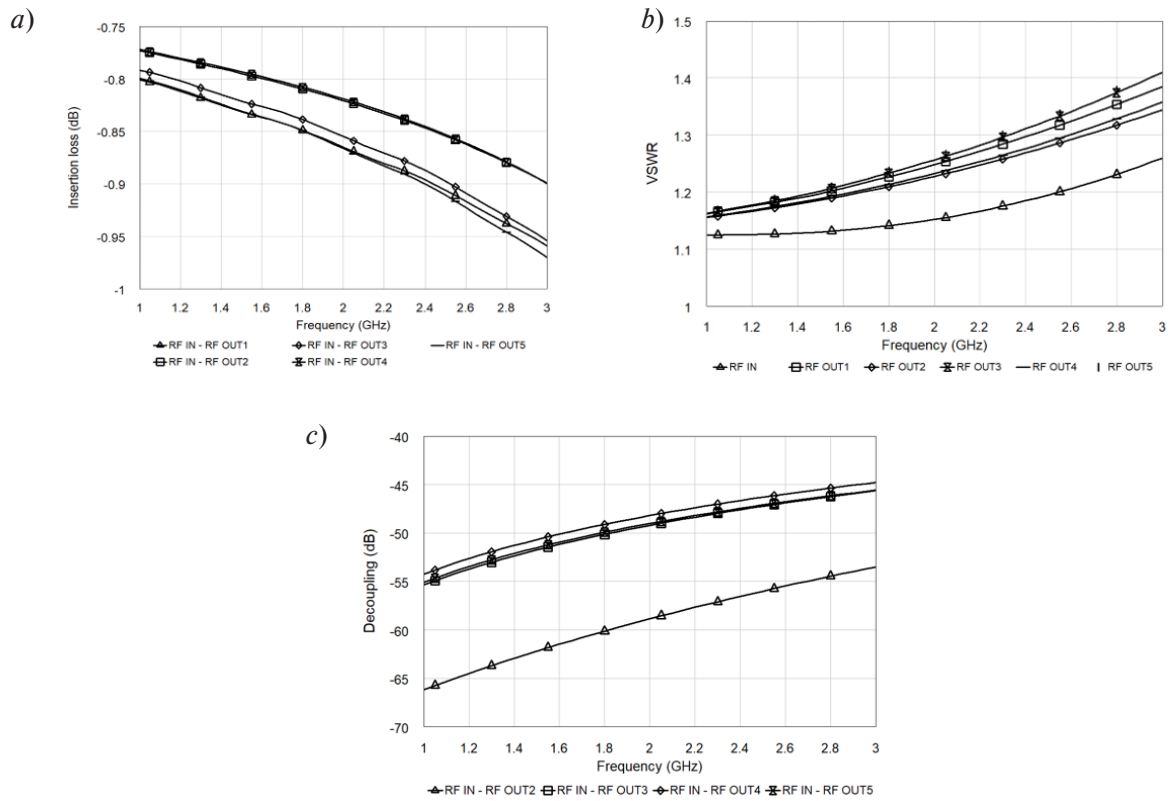


Fig. 7. Simulation results: insertion loss (a); VSWR (b); decoupling (c)

L1–L6 matches input and output of the circuit to 50Ω ($L1 = 0.68 \text{ nH}$, $L2\text{--}L6 = 0.41 \text{ nH}$). The nominal for all gate resistors is the same as for the designed 2-bit attenuator ($4.5 \text{ k}\Omega$ for $R_{g1}\text{--}R_{g10}$).

Simulation results of the designed SP5T switch are presented in Fig. 7. Insertion loss is less than 1 dB, VSWR is less than 1.5 and decoupling does not exceed -44 dB .

Front-end

The layout of the designed front-end is presented in Fig. 8. The MMIC dimensions are $3.4 \times 3.2 \text{ mm}$. The microwave outputs were spaced in such a way as to simplify the routing of the printed circuit board traces to the MMIC.

The circuit design, simulation and optimization were performed using AWR Design Environment. Electromagnetic analysis of the passive structures conducted using AXIEM simulator. The results of the analysis of the designed front-end in the small-signal mode is demonstrated in Fig. 9. Gain ($|S_{21}|$) is no less than 29.9 dB, input and output return loss ($|S_{11}|$ and $|S_{22}|$) are less than -8.4 dB and NF does not exceed 1.21 dB.

The 1 dB compression point $P_{1\text{dB}}$ of the front-end is 20.6 dB at 2 GHz and the output third intercept point OIP3 for two close frequencies is 30.1 dB. Total current consumption is less than 85 mA at 5 V.

A comparison of the results shows that the main parameters of the designed front-end are comparable to foreign analogues, and in some cases even surpasses them. For example, the Qorvo QPM2101¹ GaAs multi-chip operates over 2.5–4 GHz frequency range, has a comparable gain (30 dB typical) and superior NF (1 dB typical). It has wider gain control range (0–31.5 dB with 0.5 dB step) than the designed front-end. However, Qorvo's chip has significantly larger dimensions ($7.0 \times 7.0 \text{ mm}$), poor linearity level ($P_{1\text{dB}}$ is 14 dBm at 3.1 GHz), and total current consumption reaches 175 mA at 3.3 V.

¹ Multi-Chip T/R Module. QPM2101. [online] Available: <https://www.qorvo.com/products/p/QPM2101> (Accesses: 25.06.2026).

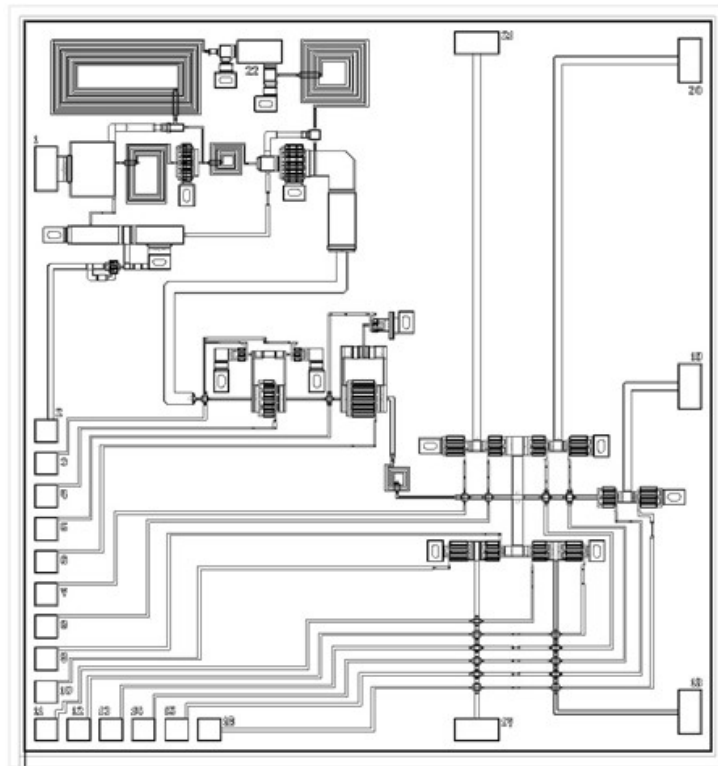


Fig. 8. Layout of front-end

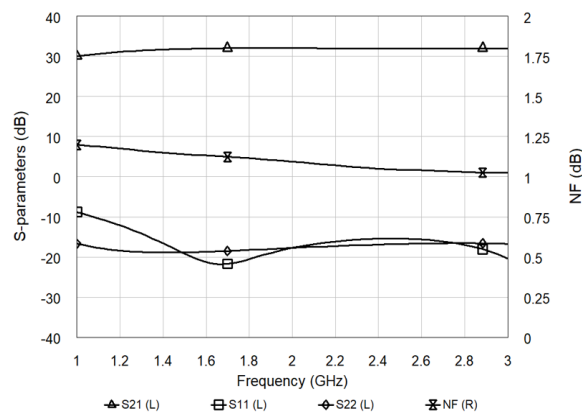


Fig. 9. S-parameters and NF of front-end

Another analogue, ADRF5549, the dual-channel front-end from Analog Devices², incorporating chips on Si and GaAs processes, has the highest gain (35 dB at 2.3 GHz), comparable NF (1.4 dB at 2.3 GHz) and linearity (P_{1dB} is 19 dBm at 2.4 GHz), but the shortest operating frequency range (1.8–2.8 GHz), poor gain control (17–35 dB with only 1 step) and larger dimensions (6.0×6.0 mm). Current consumption is the same as for the designed front-end (85 mA at 5 V).

² Receiver Front End. ADRF5549. [online] Available: <https://www.analog.com/en/products/ADRF5549.html> (Accesses: 25.06.2026).

Conclusion

As a result of this research, a multifunctional front-end for downconverter applications in the 1–3 GHz frequency range was designed using domestic GaAs pHEMT technology. The designed MMIC integrates a LNA, a 2-bit digital attenuator, and a SP5T switch on a single die, achieving a compact layout of 3.4×3.2 mm. A stage-level design methodology was proposed for the LNA, combining RC-feedback networks and optimized transistor peripheries to meet required specifications. The attenuator sections were realized using bridged T- and Π -networks, while the SP5T switch employed a series-shunt topology with a five-way combining junction to minimize chip area.

The simulated performance of the complete front-end meets all specified targets: gain is no less than 29.9 dB, NF is no more than 1.21 dB, input and output return loss better than –8.4 dB, and total current consumption below 85 mA at 5 V. The linearity figures ($P_{1dB} = 20.6$ dBm, OIP3 = 30.1 dBm) confirm its suitability for modern receiver systems.

A comparative analysis with commercial analogues (QPM2101 and ADRF5549) demonstrates that the designed MMIC offers a competitive combination of wide operating bandwidth, low noise, moderate current consumption, and compact size. While some analogues provide wider gain control ranges or slightly higher gain, they often suffer from larger dimensions, inferior linearity, or narrower frequency coverage. The proposed front-end thus represents a viable domestic alternative, highlighting the potential of local GaAs pHEMT processes for high-performance MMICs.

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