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STABILIZED CURRENT SOURCE IN 180 NM CMOS

K.A. Mironov  , *D.V. Morozov*  , *M.M. Pilipko* 

Peter the Great St. Petersburg Polytechnic University,
St. Petersburg, Russian Federation

✉ mironov.ka@edu.spbstu.ru

Abstract. This paper presents a comparative analysis of four CMOS stabilized current source architectures: the beta-multiplier, an op-amp-enhanced beta-multiplier, the Nagata current source, and a modified Nagata source with active feedback based on an op-amp. The study focuses on evaluating their performance in terms of thermal stability, dependence on supply voltage and the output noise current spectral density. Analytical considerations were validated through simulation using the Mikron JSC 180 nm 1.8 V CMOS process. The findings reveal the trade-offs between circuit complexity, supply voltage and temperature independence, as well as noise level. The op-amp-enhanced Nagata current source is the best of the considered circuits and has the following characteristics: nominal current 15.14 μA , supply voltage dependence of the reference current 0.1 $\mu\text{A/V}$, RMS output noise current 63.98 nA (within 0.1 Hz to 1 MHz band), current temperature coefficient 66.15 ppm/ $^{\circ}\text{C}$. This circuit has been chosen for the layout implementation. Layout sizes are $18 \times 28 \mu\text{m}$.

Keywords: CMOS, reference current source, output noise current, PTAT current, CTAT current

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ИСТОЧНИК СТАБИЛИЗИРОВАННОГО ТОКА ПО ТЕХНОЛОГИИ КМОП 180 НМ

К.А. Миронов , Д.В. Морозов , М.М. Пилипко 

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

 mironov.ka@edu.spbstu.ru

Аннотация. Представлен сравнительный анализ четырех архитектур стабилизированных источников тока на основе КМОП-технологии: бета-умножителя, улучшенного бета-умножителя с операционным усилителем, источника тока Нагаты и модифицированного источника Нагаты с активной обратной связью на основе операционного усилителя. Рассматриваются температурная стабильность, зависимость от напряжения питания и спектральная плотность выходного шумового тока. Проведено моделирование с использованием КМОП-технологии АО «Микрон» 180 нм 1,8 В. Представлен компромисс между сложностью схемы, зависимостью от напряжения питания и температуры, а также уровнем шума. Источник тока Нагаты с операционным усилителем является лучшей из схем и имеет следующие характеристики: номинальный ток 15,14 мкА, зависимость опорного тока от напряжения питания 0,1 мкА/В, среднеквадратичный выходной шумовой ток 63,98 нА (в диапазоне частот от 0,1 Гц до 1 МГц), температурный коэффициент тока 66,15 ppm/°C. Эта схема была выбрана для реализации топологии. Размеры топологии составляют 18 × 28 мкм.

Ключевые слова: КМОП, источник тока, спектральная плотность шумового тока, ток пропорциональный температуре, ток обратно пропорциональный температуре

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW» (FSMR-2023-0008).

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Introduction

High-precision current references are fundamental building blocks in modern CMOS integrated circuits, serving as the backbone for biasing of analog stages, data converters, and radio-frequency front-ends. As semiconductor technologies scale down to the nanometer range, the reduction in supply voltage (V_{DD}) and the increase in process variations introduce significant challenges for maintaining stable bias currents [1–3].

Among a variety of circuit solutions, the beta-multiplier current reference is widely used due to its simplicity and relative independence from supply voltage compared to basic mirrors [3]. However, the classical beta-multiplier architecture often suffers from channel length modulation and limited temperature stability. As established in [3], the integration of an operational amplifier into the beta-multiplier loop can significantly enhance supply rejection by equalizing the drain voltages of the sensing transistors, effectively isolating the output current from V_{DD} fluctuations.

The Nagata current source offers an alternative approach to stabilization [4, 5]. Originally developed to provide a current output that is relatively insensitive to input current variations, the Nagata cell utilizes a self-biasing mechanism with a nonlinear transfer characteristic. Unlike a standard current mirror, where the output current scales linearly with the input, the Nagata architecture is designed to reach a stable equilibrium point. This inherent property not only improves supply decoupling but also provides additional degrees of freedom for temperature compensation. By selecting appropriate transistor geometries and resistance values, the circuit can be tuned to minimize the overall temperature coefficient [6, 7].

This paper provides a comparison of four architectures – the classical beta-multiplier, the op-amp-enhanced beta-multiplier, the Nagata source, and the modified Nagata source – evaluating their trade-offs in terms of stability and noise level.

General considerations

Beta-multiplier

The beta-multiplier generates a current based on the transconductance asymmetry between two MOSFETs. Assuming that both MOSFETs (M1 and M2 in Fig. 1, *a*) operate in the saturation region and that the channel length modulation is negligible ($\lambda = 0$), the equation for the reference current can be derived as follows:

$$I_{out} = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L} \right)_1 R^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2, \quad (1)$$

where K is the sizing ratio factor between M2 and M1. This equation does not consider the dependence on supply voltage variation due to neglecting of λ and non-idealities of pMOSFETs-based current mirror. However, it demonstrates a fundamental limitation in current stabilization. The output current is inversely proportional to the square of the resistance R , so even small fluctuations in resistance (e.g. process corners) will significantly affect the nominal value of the output current.

To minimize the impact of supply voltage fluctuations, an op-amp is added to the beta-multiplier circuit to implement an active feedback loop. The main function of the op-amp is to equalize the drain voltages of the current-sourcing MOSFETs (M1 and M2). This feedback ensures that both branches of the circuit operate under identical V_{ds} conditions, with an accuracy inversely proportional to the op-amp gain, so the currents in the right and left branches are equal. In essence this technique helps to boost the output resistance of the pMOSFETs-based current mirror and suppress the channel length modulation effect. A similar effect can be achieved by utilizing long-channel transistors or cascode structure, although it is less efficient in terms of voltage headroom and supply rejection.

Nagata current source circuit

The Nagata current source uses a different method of current stabilization, which differs fundamentally from the ΔV_{gs} subtraction technique used in beta-multiplier. To demonstrate this, the Nagata current mirror, which is at the core of this circuit, was examined. Unlike a traditional current mirror, the gate of the output MOSFET M2 is connected to the drain of the input MOSFET M1, thereby forming a negative feedback loop. Consequently, when the input current increases, the voltage drop across resistor R begins to limit the gate potential of the output transistor, creating a non-monotonic (peaking) transfer characteristic $I_{out} = f(I_{in})$. By selecting the resistor value and the magnitude of the input and output currents appropriately, the operating point can be fixed at the peak where the sensitivity of the current to changes in the supply voltage is close to zero ($\partial I_{out} / \partial V_{dd} = \partial I_{out} / \partial I_{in} = 0$). This circuit solution can be used in technologies lacking complementary devices (e.g. GaAs MMICs). In such cases, it is impossible to create a pMOSFETs-based current mirror for power

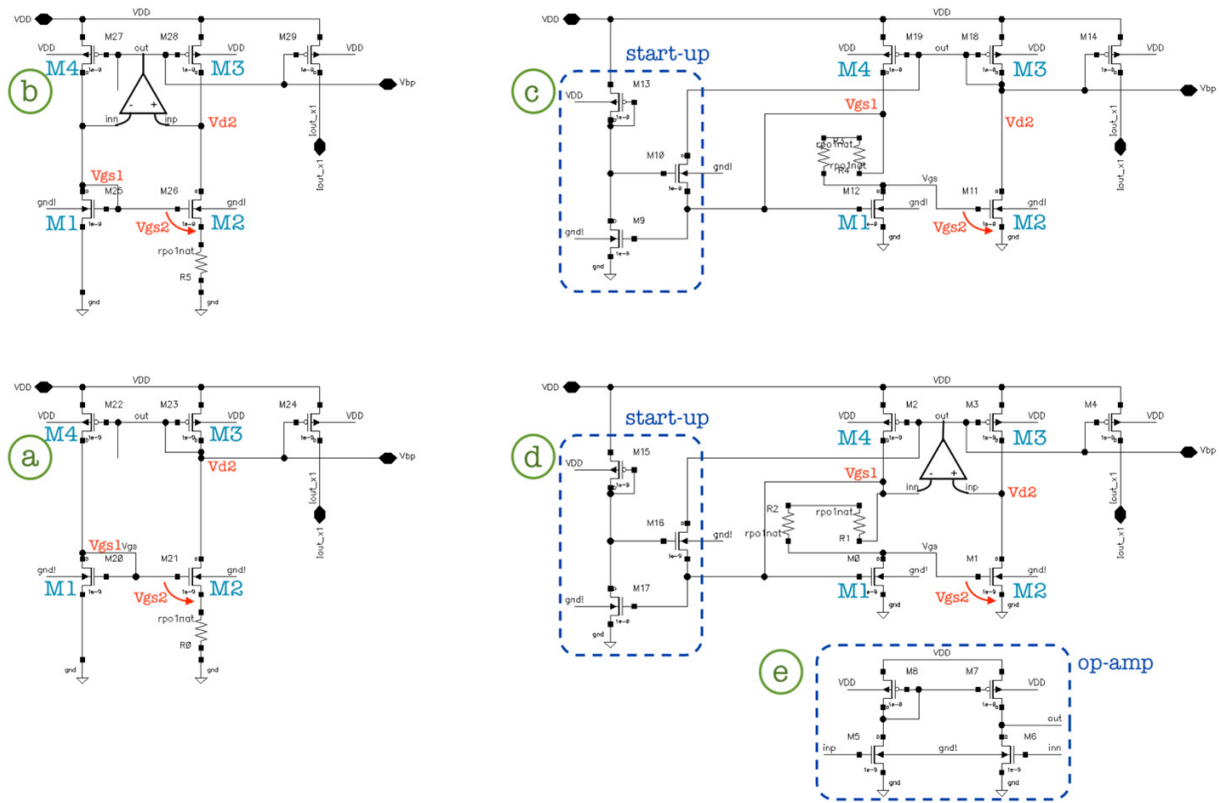


Fig. 1. Stabilized reference current source circuits: beta-multiplier (a); op-amp-enhanced beta-multiplier (b); self-biased Nagata circuit (c); op-amp-enhanced Nagata circuit (d); op-amp circuit (e)

decoupling nor can an op-amp be used to equalize the voltages at the transistor drains. The Nagata circuit is one of the few that allows the output current to be stabilized with respect to the supply voltage.

In contemporary CMOS circuit design, an active load in the form of a pMOSFETs-based current mirror is used to ensure branch current balancing and power supply decoupling. Using resistors as a load is impractical in CMOS designs because generating microampere-range currents requires resistances of around 100 kΩ. Even when high-resistance polysilicon resistors are used, they occupy a significantly larger area than the rest of the circuit. When using an active load in the form of a pMOSFETs-based current mirror, an additional positive feedback loop is formed. Let us examine the feedback in the Nagata circuit in more detail to understand the main difference from the beta-multiplier circuit.

Supply voltage dependence

In a self-bias circuit, there are two feedback loops: a negative feedback loop (comprising MOSFETs M1, M2, and a resistor R) and a positive feedback loop (implemented as a pMOSFETs-based current mirror). Positive feedback allows the output current of MOSFET M2 to be linked to the input current of MOSFET M1. As the current through M2 changes, the input current of M1 changes in the same way. Negative feedback operates similarly to a Nagata current mirror: as the current through M1 increases, the voltage drop across resistor R increases. This reduces $V_{ds1} = V_{gs2}$, which in turn reduces the current through M2 and subsequently leads to a reduction in the current through M1 via the current mirror. Thus, the combination of positive and negative feedback loops creates self-bias and brings the circuit to a state of stable equilibrium. However, a side effect is the need for a startup circuit, which is required to ensure the correct functioning of the circuit. It is important to note that

the loop gain in the Nagata circuit is significantly greater than in the beta-multiplier circuit. In the Nagata circuit, changes in the input current (through MOSFET M1) are transmitted to the gate of MOSFET M2 via the voltage drop across the resistor. This causes a significant change in the current through M2, which is proportional to the transfer conductance. The open-loop gain is determined by equation

$$LG_N = 1 - g_{m1} \cdot R. \quad (2)$$

It is important to note that the open-loop gain is negative, with a magnitude of 15 for 180 nm CMOS process.

In the beta-multiplier circuit, a change in the input current does not directly affect the V_{gs2} voltage, but rather through the source degeneration negative feedback. This provides milder feedback, which changes the current in the output branch smoothly until a steady-state equilibrium of the input and output currents is reached. The open-loop gain is described by formula

$$LG_\beta = \frac{g_{m2}/g_{m1}}{1 + g_{m2} \cdot R} \quad (3)$$

and, unlike Nagata's, it is positive and relatively small (~ 0.2 for 180 nm CMOS process).

Let us consider the dependence of the bias current on the supply voltage. Although the pMOS-FETs-based current mirror is intended to provide supply decoupling, the dependence of the reference current on the supply voltage remains significant due to the strong influence of channel length modulation in short-channel transistors. When the supply voltage changes, the gate voltage of MOSFET M1 changes too, leading to a change in the reference current. For simplicity, therefore, we will base our further discussion on V_{gs1} rather than V_{dd} , assuming that they are related via the dependence $I_{d_pMOS}(V_{ds})$. While both circuits have an output resistance equal to $1/g_{m1}$ at the V_{gs1} node, the critical output resistance is that of the current-sourcing MOSFET, which is M2 in both circuits. In the beta-multiplier circuit, the output resistance is determined by the feedback resistor (source degeneration) according to expression

$$R_{out\beta} = r_{ds2} \cdot (1 + g_{m2} \cdot R) + R. \quad (4)$$

In the Nagata circuit, the output resistance of the current-sourcing transistor is equal to r_{ds2} , resulting in a stronger dependence of the reference current on the supply voltage.

In the case of MOSFETs with a channel length of $1...3 \cdot L_{min}$, the channel length modulation effect is significant, potentially resulting in a supply voltage dependence of up to 30 %/V. Therefore, the use of op-amp-enhanced architectures is highly recommended for use with short-channel technologies. By incorporating an active gain stage that forces the drain potentials of the transistor pair to be identical, the circuit effectively isolates the reference core from external voltage fluctuations. This architectural modification converts the source-degenerated branch into a regulated cascode structure, where any error signal caused by V_{dd} variation is amplified by the open-loop gain A_v of the op-amp before being applied to the gate of the regulating transistor, thereby counteracting the change. The quantitative advantage of this active regulation can be estimated by multiplying the output resistance by a value of $(1 + A_v)$ which, for 180 nm CMOS process, can exceed 20. Despite these advantages, using of the op-amps can increase the output noise current.

Thermal stability

Classical solutions

The simplest method of achieving temperature insensitivity is to bias the current-sourcing MOSFET at its Zero Temperature Coefficient ($V_{gs} = V_{ZTC}$) operating point (Fig. 2, *a*) [8]. This arises from the mutual compensation of two temperature-dependent mechanisms: carrier mobility (μ) and threshold voltage (V_{th}). At low V_{gs} levels (near the subthreshold region), the drain current exhibits a positive temperature coefficient, primarily due to the reduction in V_{th} as temperature rises. Conversely, at higher V_{gs} levels in strong inversion, mobility degradation becomes the dominant factor, resulting in a negative temperature coefficient for the drain current. At the specific bias point $V_{gs} = V_{ZTC}$, these competing effects introduce equal and opposite changes, ensuring that the drain current remains stable over a certain temperature range. However, this approach is highly sensitive to external variations. Any process corner shifts or V_{dd} fluctuations significantly displace the V_{ZTC} point, leading to significant degradation the circuit thermal stability.

Circuit designs based on bandgap circuits are among the most precise methods of generating a thermally stable current [9, 10]. This approach is based on the sum of currents with opposite temperature coefficients (Fig. 2, *b*) according to the expression

$$I_{ref} = \alpha \cdot I_{PTAT} + \beta \cdot I_{GTAT}, \quad (5)$$

where α and β are the proportionality coefficients. A typical circuit diagram of such reference source is shown in Fig. 2, *c*. The output current component IPTAT (Proportional To Absolute Temperature) has a positive temperature coefficient and can be implemented using a bandgap circuit with bipolar transistors. The second component, I_{GTAT} (Complementary To Absolute Temperature), has a negative temperature coefficient and the possible realizations are a single current-sourcing bipolar transistor or beta-multiplier.

This approach has drawbacks. When mixing currents, only the first-order temperature derivatives of the current can be compensated. All second-order effects continue to influence the system, resulting in a parabolic rather than constant temperature dependence. Additionally, due to the presence of multiple current paths (requiring two: CTAT and PTAT sources) increases noise, power consumption and die area. However, it is worth noting that using a bandgap circuit as the I_{PTAT} current source should reduce the variation in the reference current parameters due to corner deviations and mismatch, because the bipolar transistors used as current-sourcing elements in such a circuit have very small variations across corners and mismatch.

Beta-multiplier thermal stability

The beta-multiplier architecture is fundamentally limited to a monotonic temperature response. Even by adjusting the temperature coefficient of the resistor, it is nearly impossible to achieve temperature compensation. This limitation arises from the circuit feedback loop gain: the source degeneration resistor R forces the currents in both branches to change synchronously. Consequently, even if transistors are biased at different points relative to their V_{ZTC} in order to cancel out thermal effects, the feedback mechanism ensures that any temperature-induced variation alters the current in both branches equally. This synchronization preserves the core linear temperature dependence and prevents flexible adjustment of the temperature coefficient. The only degree of freedom is that M1 and M2 can be biased above or below V_{ZTC} thereby producing a positive or negative temperature coefficient. For typical transistor sizes the operation point is above V_{ZTC} , which causes a CTAT current. In order to create PTAT current, both MOSFETs should be biased below the VZTC voltage, which requires significant increase in W/L to raise the V_{ZTC} . However, this result is not stable because V_{ZTC} changes dramatically with process variations.

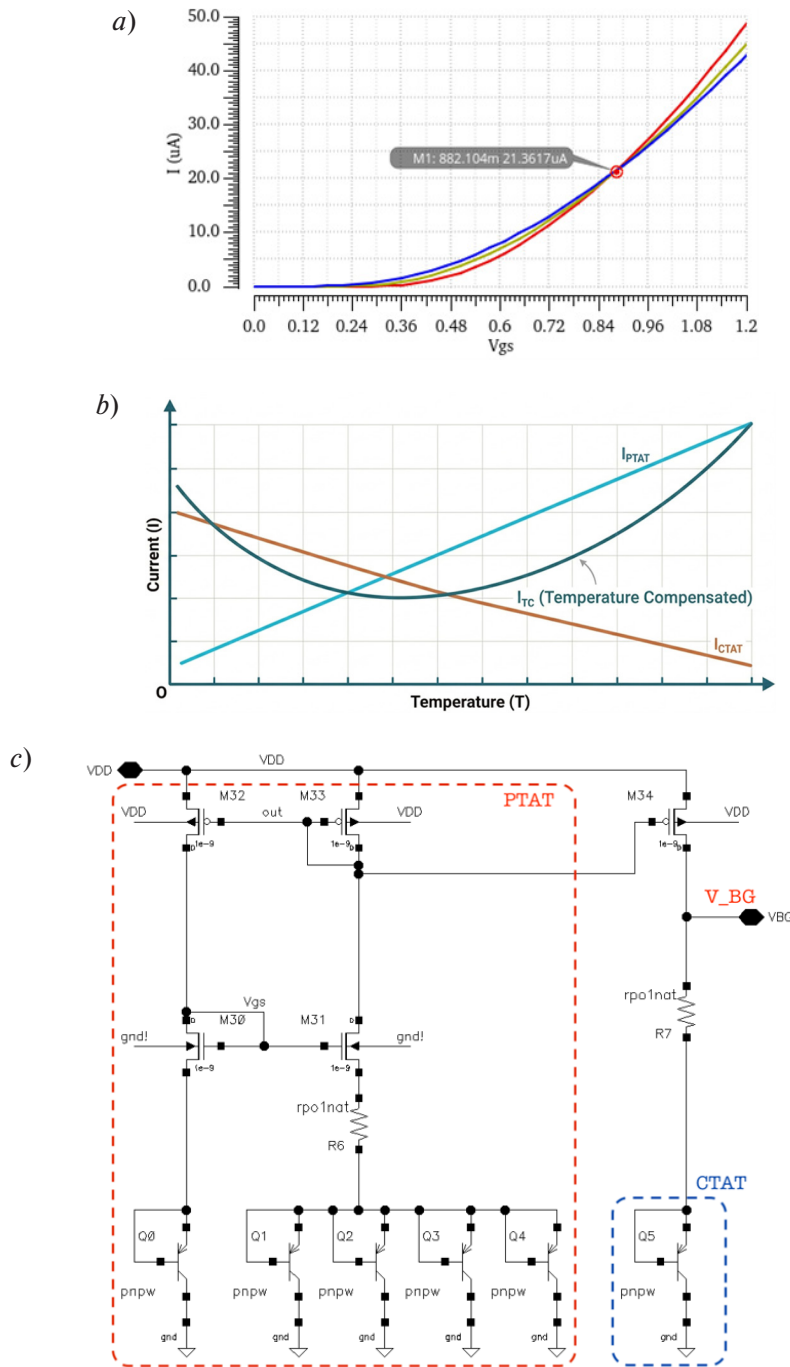


Fig. 2. Zero temperature coefficient voltage V_{ZTC} (a); concept of generating a thermally stable current by combining PTAT and CTAT currents (b); possible bandgap circuit solution (c)

Nagata circuit thermal stability

The temperature stabilization mechanism in the Nagata current source can be explained by analyzing the dynamic balance within its self-biased loop. Let us assume that both MOSFETs M1 and M2 are biased below their V_{ZTC} point, meaning their drain currents inherently exhibit a PTAT characteristic due to the dominant influence of the threshold voltage shift ($\partial V_{th} / \partial T$). Furthermore, the polysilicon resistor R possesses a negative temperature coefficient, which also contributes to a potential current increase as temperature rises.

As temperature increases, the current through M1 tends to rise due to its positive temperature coefficient. This current increment increases the voltage drop across the resistor R . According to the loop gain equation, this reduces the gate-source voltage of M2. Specifically, the change in V_{gs2} is governed by the relation

$$V_{gs1} = V_{gs2} + I_{ref} R. \quad (6)$$

Since the resistance R decreases with temperature, the loop gain slightly decreases causing less effective regulation. In other words, the rise in M1 current acts to suppress the current flowing through M2. However, since M2 is also a PTAT current generator, this suppression is partially cancelled by the own thermal sensitivity of M2. Anyway, the correction signal (current) formed by this loop is fed back to M1 via the pMOSFETs-based current mirror, ultimately stabilizing the reference current.

It is important to note that while the temperature coefficient of the resistor plays a role, it is not the primary driver of the temperature insensitivity. The core stabilization arises from the different thermal sensitivity between M1 and M2. According to the loop equation (6), MOSFET M1 always operates at a higher inversion level (higher current density) than M2. Consequently, even though both are biased below V_{ZTC} , the current in M2 is significantly more sensitive to temperature variations due to the stronger relative influence of V_{th} at lower current densities.

By meticulously optimizing the MOSFET geometries (W/L ratios), these competing thermal increments can be tuned. This leads to a non-monotonic, parabolic temperature dependence of the reference current I_{ref} , characterized by an extremum point where $\partial I_{ref} / \partial T = 0$.

It was originally assumed that the operating voltages of MOSFETs M1 and M2 would be below V_{ZTC} . However, it is also acceptable for MOSFET M1 to be near V_{ZTC} , even if slightly above it. This can, however, lead to the following problem. If V_{gs1} rises significantly above the thermally stable point, the feedback loop in the Nagata circuit will be unable to overcome the CTAT behavior of MOSFET M1, and the circuit will lose its thermal stability.

Since V_{gs1} is significantly higher than V_{gs2} , it is difficult to shift M1 below V_{ZTC} and keep M2 in saturation. To achieve this, the MOSFET geometry must be modified to increase the V_{ZTC} voltage. Experimental findings indicate that the MOSFET channel length has the greatest impact on the V_{ZTC} voltage, with a decrease observed as the channel length increases. To illustrate, when the channel length increases from 0.18 to 2 μm , the voltage V_{ZTC} decreases from 750 to 660 mV. Since both MOSFETs M1 and M2 must be shifted below the V_{ZTC} point ($V_{gs1} < V_{ZTC1}$ and $V_{gs2} < V_{ZTC2}$) then for the correct setting of the operating points we need to ensure that $L_1 < L_2$. The width should also be smaller, although not necessarily in the same proportion, in order to maintain equal currents in both branches.

Simulation results

To verify the theoretical considerations, simulations were performed using the Mikron JSC 180 nm CMOS process. The paper analyzes four circuits: the classical beta-multiplier and Nagata current source circuit, as well as their op-amp-enhanced versions (Fig. 1). To ensure an objective comparison, all circuits were designed with a nominal current of 15 μA and with comparable lengths and widths of the nMOSFETs and pMOSFETs in both the Nagata and beta-multiplier circuits.

Figs. 3–4 show simulation results, which demonstrate dependencies on temperature and supply voltage. Fig. 5 depicts the output noise current spectral densities.

Comparison

Table 1 summarizes the simulation results of four considered circuits. As seen, implementations that use a simple current mirror as the self-bias circuit are significantly dependent on the supply voltage (4.7 $\mu\text{A/V}$ for the beta-multiplier and 2.3 $\mu\text{A/V}$ for the Nagata circuit, 31 and 15 %/V, respectively,

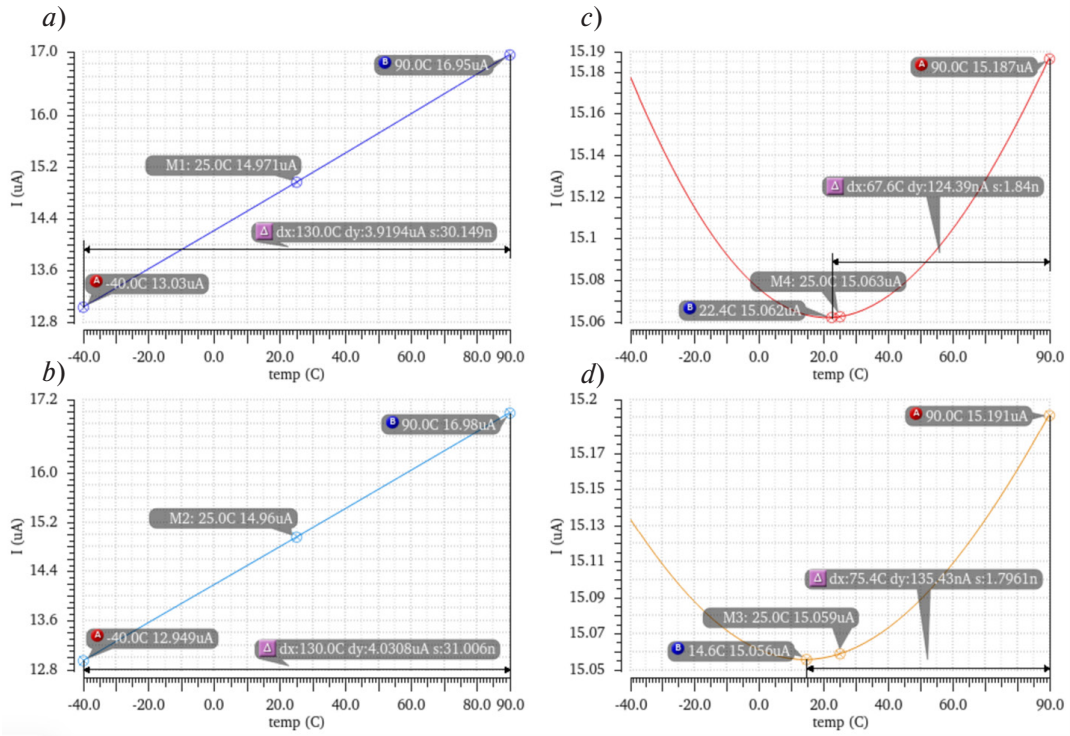


Fig. 3. Temperature dependences of the reference current for (a) classical beta-multiplier current source, (b) op-amp-enhanced beta-multiplier, (c) self-biased Nagata current source, (d) op-amp-enhanced Nagata circuit

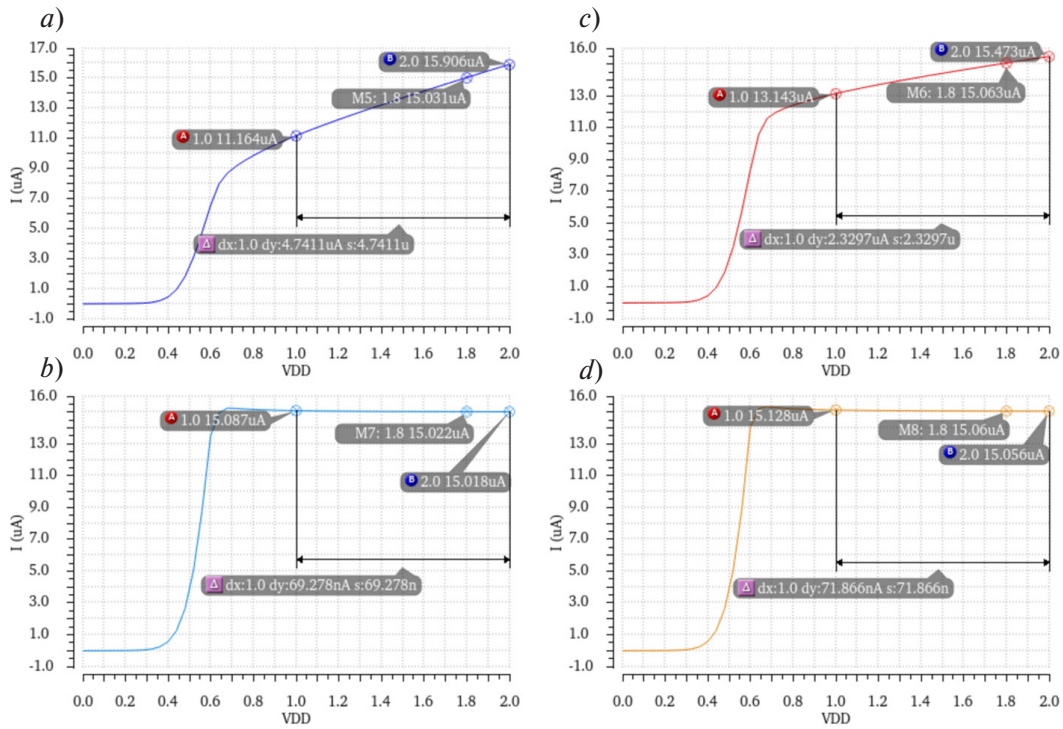


Fig. 4. Supply voltage dependences of the reference current for (a) classical beta-multiplier current source, (b) op-amp-enhanced beta-multiplier, (c) self-biased Nagata current source, (d) op-amp-enhanced Nagata circuit

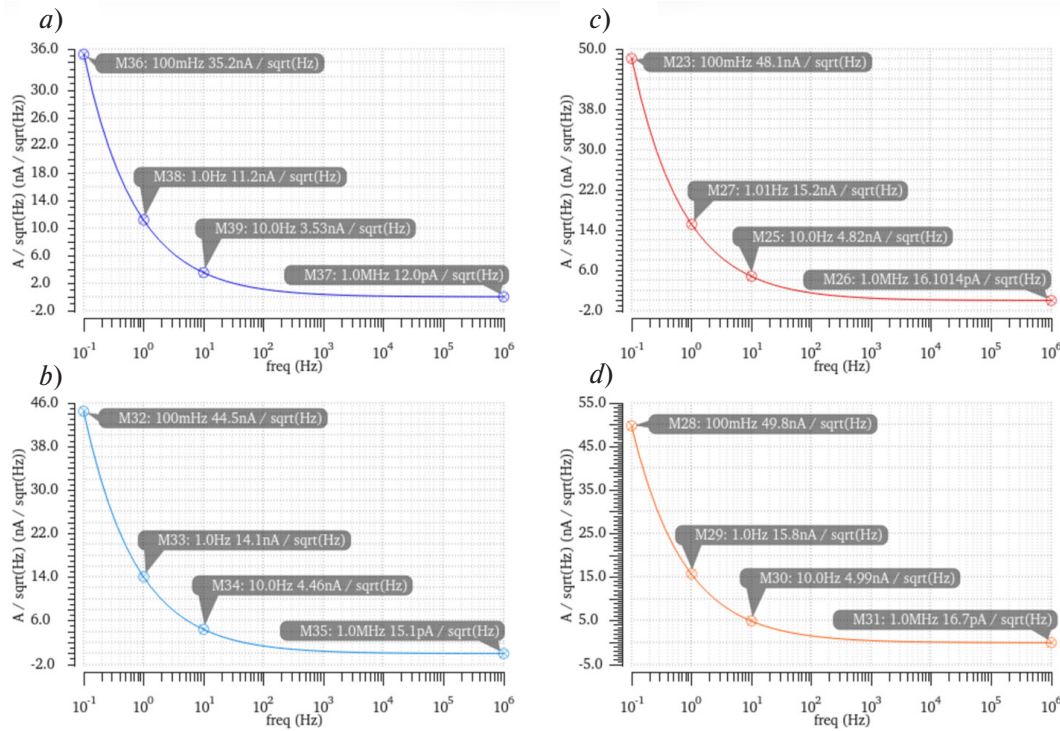


Fig. 5. Reference current noise spectral density for (a) classical beta-multiplier current source, (b) op-amp-enhanced beta-multiplier, (c) self-biased Nagata current source, (d) op-amp-enhanced Nagata circuit

relative to the nominal value). Although both circuits have poor supply decoupling, the RMS value of the output noise current of the Nagata circuit is 62 nA, which is higher but comparable to that of the beta-multiplier circuit where the output noise current is 45 nA RMS.

Table 1

Comparison of the results

	Beta-multiplier (Fig. 1a)	Op-amp-enhanced beta-multiplier (Fig. 1b)	Self-biased Nagata current source (Fig. 1c)	Op-amp-enhanced Nagata current source (Fig. 1d)
Nominal current	15.11 μA	15.1 μA	15.14 μA	15.14 μA
Supply voltage dependence of the reference current (% from nominal value)	4.74 $\mu\text{A/V}$ (31.37%)	0.1 $\mu\text{A/V}$ (0.66%)	2.32 $\mu\text{A/V}$ (15.32%)	0.1 $\mu\text{A/V}$ (0.66%)
RMS output noise current (within 0.1 Hz to 1 MHz band)	45.31 nA	57.22 nA	61.82 nA	63.98 nA
Current temperature dependence (% from nominal value)	3.92 μA (26%)	4.03 μA (26.8%)	0.12 μA (0.79%)	0.13 μA (0.86%)
Current temperature coefficient	2000 ppm/ $^{\circ}\text{C}$	2060 ppm/ $^{\circ}\text{C}$	60.77 ppm/ $^{\circ}\text{C}$	66.15 ppm/ $^{\circ}\text{C}$

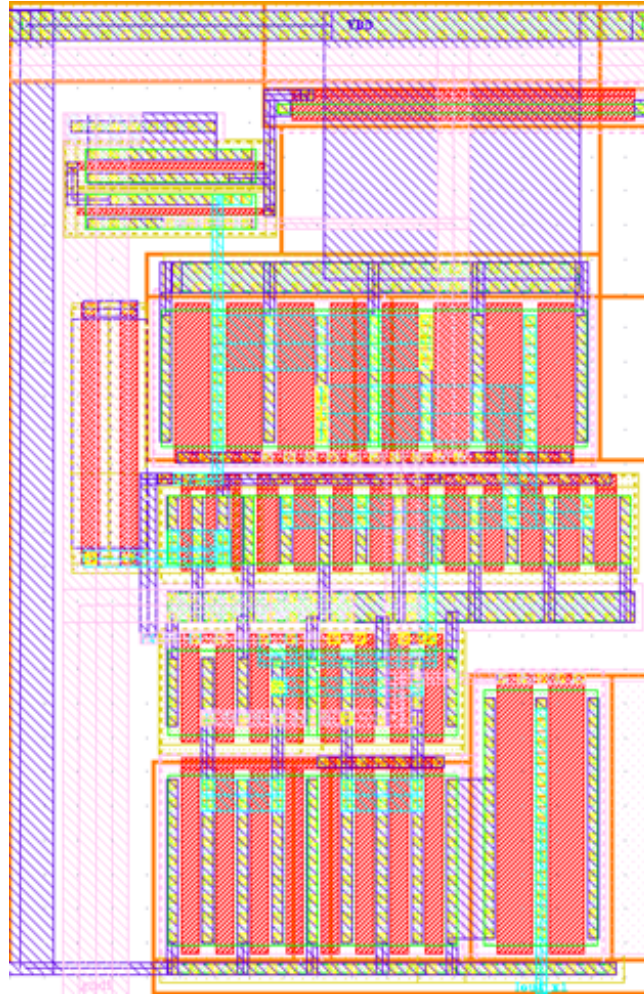


Fig. 6. Layout of the op-amp-enhanced Nagata current reference core

Using a simple four-MOSFETs op-amp provides power decoupling. The dependence on the supply voltage is $0.1 \mu\text{A/V}$ for the beta-multiplier and $0.1 \mu\text{A/V}$ for the Nagata circuit, which is 0.6 and 0.5 %/V of the nominal value, respectively. However, the op-amp-enhanced versions of both circuits have worse noise characteristics but the RMS values for the Nagata circuit and for the beta-multiplier became closer to each other.

The output current of the beta-multiplier has a positive temperature coefficient and remains constant regardless of the selected operating points of the MOSFETs. As expected, the temperature coefficient is $2000 \text{ ppm/}^\circ\text{C}$ (within the typical operating range of -40°C to $+85^\circ\text{C}$). The temperature dependence of the Nagata circuit depends significantly on the choice of operating points and MOSFETs dimensions and, for the two presented modifications equals to 61 and $66 \text{ ppm/}^\circ\text{C}$.

From the comparison in Table 1, the op-amp-enhanced Nagata current source has the best overall characteristics. Thus, it has been chosen for the layout implementation which is shown in Fig. 6. Layout sizes are $18 \times 28 \mu\text{m}$.

Conclusion

The developed reference current source circuit based on the Nagata design achieves a zero-temperature-coefficient output current behavior at the target operating temperature, providing a robust CMOS-only alternative to traditional reference architectures. Simultaneously, the Nagata current

source is more power-efficient due to its simple architecture. Unlike traditional bandgap reference circuits, which require multiple auxiliary branches to generate and then combine the PTAT and CTAT current components, the Nagata topology provides temperature compensation within a single primary current loop. By eliminating the additional current paths and summing amplifiers typically found in bandgap reference architectures, the Nagata source minimizes the total current consumption.

The results of the comparison show that the Nagata circuit has advantages in all parameters except noise, where the beta-multiplier circuit has a slightly lower value due to its different feedback loop structure. Opting for a Nagata architecture necessitates a conscious design trade-off, prioritizing thermal stability over the spectral purity of the output current.

Therefore, the use of the op-amp-enhanced Nagata current source is a promising alternative to the widely used op-amp-enhanced beta-multiplier. For a typical 180 nm CMOS process with a rated current of around 15 μA , the current versus temperature sensitivity is 66 ppm/ $^{\circ}\text{C}$, the current versus supply voltage response is 0.1 $\mu\text{A/V}$ and the RMS noise current is 64 nA. Despite a minor disadvantage in RMS output noise current (ca. 12%), the current temperature coefficient of the Nagata circuit is about 30 times better than that of the beta-multiplier.

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INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Kirill A. Mironov

Миронов Кирилл Александрович

E-mail: mironov.ka@edu.spbstu.ru

ORCID: <https://orcid.org/0009-0001-8226-6288>

Dmitry V. Morozov

Морозов Дмитрий Валерьевич

E-mail: dvmorozov@inbox.ru

ORCID: <https://orcid.org/0000-0003-3403-0120>

Mikhail M. Pilipko

Пилипко Михаил Михайлович

E-mail: m_m_pilipko@rambler.ru

ORCID: <https://orcid.org/0000-0003-3813-6846>

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