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REDUCED VOLTAGE STRESS CLASS E POWER AMPLIFIER OPERATING A COMPLEX IMPEDANCE LOAD: A PERFORMANCE ANALYSIS

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Abstract. Class E power amplifiers (PAs) attract the interest of experts involved in the development of communication and telecommunications equipment due to their high efficiency. However, the high voltage stress across transistors, which exceeds the supply voltage by 3.6–4 times, limits the output power of such amplifiers. An alternative to solve this issue could be a PA in which the peak voltage across transistor is reduced by 2 times, but still maintains the main advantages of traditional Class E, such as zero-voltage switching (ZVS) and zero-derivative voltage switching (ZDVS). In well-known publications, the study of the characteristics of PAs with lower voltage across transistors is limited to the particular case of a real impedance load. However, this condition may not be true when the PA operates in a frequency band, which will inevitably lead to errors in calculating their characteristics. The objective of the paper is to develop an analytical model of Class E PA with reduced voltage stress when operating with complex impedance load. The adequacy of the analytical model is confirmed by simulation, which shows that the relative error in the calculation of the main characteristics of the PA does not exceed 6.5%. The issues of synthesizing a filtering and matching circuit have been considered that ensures expansion of the frequency band at specified rated values in output power and voltage stress in transistor turned-on moment.

Keywords: power amplifier, class E, switching power losses, complex impedance load, harmonic balance method

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ХАРАКТЕРИСТИКИ УСИЛИТЕЛЯ МОЩНОСТИ КЛАССА Е С ПОНИЖЕННЫМ НАПРЯЖЕНИЕМ НА ТРАНЗИСТОРАХ ПРИ РАБОТЕ НА КОМПЛЕКСНУЮ НАГРУЗКУ

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Аннотация. Усилители мощности (УМ) класса Е вызывают интерес у специалистов, занимающихся разработкой аппаратуры связи и телекоммуникаций благодаря высокому КПД. Однако высокое пиковое напряжение на транзисторах, превышающее напряжение питания в 3,6...4 раза, ограничивает выходную мощность таких усилителей. Альтернативой этим устройствам могут стать УМ класса Е с пониженным напряжением на транзисторах, у которых максимальное напряжение на транзисторах снижено в 2 раза, но при сохраняются основные достоинства режима класса Е, такие как ZVS и ZVDS. В известных публикациях исследование характеристик УМ с пониженным напряжением на транзисторах ограничивается случаем нагрузки с вещественным импедансом. Однако данное условие нарушается при работе УМ в полосе частот, что неизбежно приведет к погрешности при расчете характеристик УМ. Целью настоящей публикации является разработка аналитической модели, позволяющей определить характеристики УМ в общем случае при работе на нагрузку с комплексным импедансом. В работе представлены результаты проверки достоверности аналитической модели, которая позволила установить, что ее погрешность не превышает 6,5%. Рассмотрены вопросы синтеза согласующей цепи, обеспечивающей расширение полосы частот УМ при заданных допустимых значениях непостоянства выходной мощности и скачка напряжения на транзисторах в момент коммутации.

Ключевые слова: усилитель мощности, класс Е, коммутационные потери мощности, нагрузка с комплексным импедансом, метод гармонического баланса

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Introduction

Improving power efficiency and weight and size parameters of radio transmitters can be achieved by using switched-mode power amplifiers (PAs). However, without a significant decrease in switching power losses, it doesn't guarantee achieving high efficiency. Therefore, in recent years there has been great interest in the study of PAs operating in classes DE and E where, under certain conditions, it is possible to ensure *zero-voltage-switching* (*ZVS*) and *zero-derivative-voltage-switching* (*ZDVS*), thus eliminating switching losses and insuring high efficiency [1–3].

Compared to Class DE, Class E PAs demonstrates distinct advantages:

1) higher operating frequency;
2) noticeably easier formation of signals to drive transistors.

Class E PAs lose to their competitors is in more intense operating conditions of the transistors: if in Class DE PAs the peak voltage across transistors is equal to the supply voltage, then in Class E PAs it increases by 3.6–4 times.

Proceeding from the above, when designing a PA with increased output power, the circuit considered in [4, 5] is of great interest. On the one hand, it has all the advantages of a Class E PA, and on the other

hand, it has a lower transistor voltage stress at least as much as 2 times. When analyzing the characteristics of this PA, the authors limited themselves to considering only a particular case of a resistive load. However, when the transmitter operates in a frequency band, this condition is violated, which will inevitably lead to errors in the obtained results.

Taking into account the said above, the objective of the research presented in the paper was to develop an analytical model of a Class E PA with reduced voltage stress on transistors (for the sake of abbreviation, we will further designate this Class as EV), while operating on a complex impedance load and to determine its main characteristics.

Analytical model of Class EV PA with a complex impedance load

The schematic of Class E_V PA is shown in Fig 1, *a*, which consists of transistors $VT1$, $VT2$; inductors L_1, L_2 and a complex impedance load $Z = R + jX$. To simplify a theoretical analysis, the following assumptions were introduced:

1. The transistors' on-state resistance is close to zero, and their switching time is negligible compared to the output oscillation period.
2. The output transistors' capacitance does not depend upon the drain-to-source voltage and has a constant value.
3. Losses in coils are considered negligible.
4. The inductances L_1, L_2 are the same and equal to $L/2$.
5. Given the use of a filter at the PA output for higher-harmonic suppression, the sinusoidal approximation for the load Z (Fig.1, *a*) current waveform can be applied [6–8]:

$$i_0 = I_m \sin\left(\omega t + \varphi\right),$$

with unknown amplitude I_m and initial pharse φ can be determined during analysis (Fig. 1, *b*).

Based on the above assumptions, the analysis of the processes in PA can be implemented using the equivalent circuit shown in Fig. 1, *b*, replacing transistors with switches $S1$, $S2$ with capacitors in parallel $C_1 = C_2 = C$.

Let's consider the steady-state operating mode of the circuit and assume that in the time interval $0 < \omega t \leq \pi$ the upper transistor is in the on-state (the switch $S1$ is closed), and the lower transistor, accordingly, is in the off-state. Then applying in the circuit in Fig. 1, *b* Kirchhoff's current and voltage laws, one can compose a system of equations:

a) *b*)

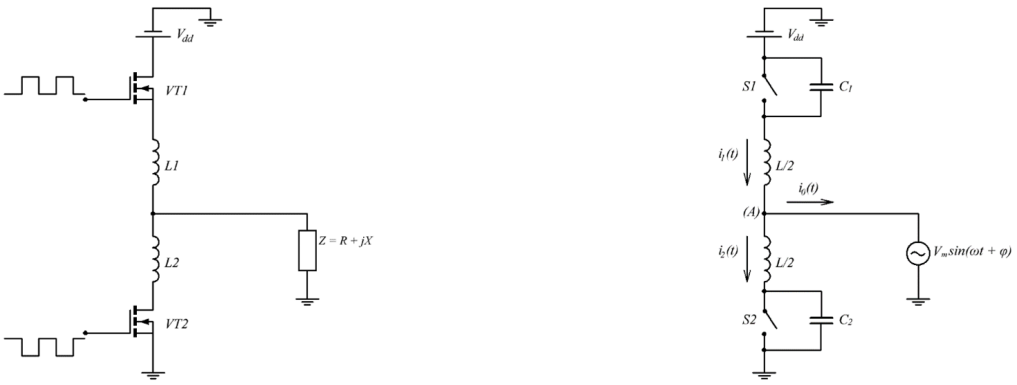

Fig. 1. PA Class E_V: functional circuit (*a*); equivalent circuit (*b*)

$$\begin{cases} V_{dd} = \upsilon_{L1}(t) + \upsilon_{L2}(t) + \upsilon_{C2}(t) & (1) \\ i_1(t) = i_2(t) + i_0(t) & (2) \end{cases},$$

where V_{dd} – supply voltage; $\upsilon_{L1}(t)$, $\upsilon_{L2}(t)$, $\upsilon_{C2}(t)$, – voltage across inductors L_1, L_2 and output capacitor transistor C_2.

Solving (1), (2) together, after necessary transformations we get the voltage across transistor $VT2$ during the time interval $0 < \omega t \le \pi$:

$$\begin{gathered} \upsilon_2(\theta) = \pi\nu\sin(\nu\theta) - \nu I_0 \sin\varphi\sin(\nu\theta) + 1 - \cos(\nu\theta) + \\ + \frac{\nu I_0 \sin\varphi}{2(1-\nu^2)}\sin(\nu\theta) - \frac{\upsilon^2 I_0 \sin\varphi\sin\theta}{2(1-\nu^2)} - \frac{\nu^2 I_0 \cos\varphi}{2(1-\nu^2)}\left[\cos(\nu\theta) - \cos\theta\right], \end{gathered} \tag{3}$$

where

$$\begin{cases} \nu = \dfrac{\omega_0}{\omega} = \dfrac{1}{\omega\sqrt{LC}}, \\ \theta = \omega t, \\ I_0 = \dfrac{\omega L I_m}{V_{dd}} \\ \upsilon_2(\theta) = \dfrac{\upsilon_{C2}(\theta)}{V_{dd}}. \end{cases} \tag{4}$$

The current through $VT1$ at the time interval $0 < \omega t \le \pi$, when $S1$ is in the on-state, is given by:

$$\begin{gathered} i_1(\theta) = \frac{\pi\cos(\nu\theta)}{I_0} + \frac{\sin(\nu\theta)}{I_0\nu} - \sin\varphi\cos(\nu\theta) + \frac{\nu\cos\varphi\sin(\nu\theta)}{2(1-\nu^2)} - \\ - \frac{\cos\varphi\sin\theta}{2(1-\nu^2)} + \frac{\sin\varphi}{2(1-\nu^2)}\left[\cos(\nu\theta) - \cos\theta\right] + \sin(\theta+\varphi). \end{gathered} \tag{5}$$

Similarly, during the time interval $\pi < \theta \le 2\pi$ when $S2$ is off-state, the voltage and the current through the lower transistor $VT2$ satisfy relations:

$$\begin{gathered} \upsilon_1(\theta) = \pi\nu\sin(\nu\theta) + I_0\sin\varphi\sin(\nu\theta) + 1 - \cos(\nu\theta) - \\ - \frac{\nu I_0\sin\varphi}{2(1-\nu^2)}\sin(\nu\theta) + \frac{\nu^2 I_0\sin\varphi\sin\theta}{2(1-\nu^2)} + \frac{\nu^2 I_0\cos\varphi}{2(1-\nu^2)}\left[\cos(\nu\theta) - \cos\theta\right]; \end{gathered} \tag{6}$$

$$\begin{gathered} i_2(\theta) = \frac{\pi\cos(\nu\theta)}{I_0} + \frac{\sin(\nu\theta)}{I_0\nu} + \sin\varphi\cos(\nu\theta) - \frac{\nu\cos\varphi\sin(\nu\theta)}{2(1-\nu^2)} + \\ + \frac{\cos\varphi\sin\theta}{2(1-\nu^2)} - \frac{\sin\varphi}{2(1-\nu^2)}\left[\cos(\nu\theta) - \cos\theta\right] - \sin(\theta+\varphi). \end{gathered} \tag{7}$$

The unknown parameters φ and I_0 can be determined using relations (3) and (6). The investigation concentrates on the practically important "soft- switching", where transistor switching occurs under both *ZVS* (*zero voltage switching*) and *ZVDS* (*zero voltage derivative switching*) [7, 9–11]. The first condition ensures that the output capacitance is completely discharged before turn-on (typical for Class E PA), resulting in zero switching losses. The second condition assumes that the derivative of the voltage on the transistor output capacitance is equal to zero, which means that there is no current when the switching starts. This condition is necessary to eliminate voltage surges in parasitic inductances and due to that to reduce high-frequency oscillations.

The analytical solutions for φ(ν) and $I_0(\nu)$ are represented in Table 1.

Table 1

The analytical solutions

$\nu = \frac{\omega_0}{\omega}$	0.8	0.9	1.0	1.1	1.2	1.3	1.4
φ, deg	–35.8	–36.9	–38.2	–39.7	–41.5	–43.8	–49.7
$I_0 = \frac{\omega L I_m}{V_{dd}}$	3.7	2.7	2.0	1.6	1.2	0.9	0.7

Fig. 2 displays the normalized voltage waveforms across transistor capacitances $\left(\upsilon_1(\theta),\ \upsilon_2(\theta)\right)$ and corresponding current waveforms $\left(i_1(\theta),\ i_2(\theta)\right)$ as functions of phase angle θ, calculated for various frequency parameter ν values.

As shown in Fig. 2, the capacitor voltage waveforms and transistor currents both satisfy the "*soft-switching*" conditions. At the same time, the voltage stress on transistor is approximately 2 times less than that of PA Class E. This allows increasing the output power compared to the Class E PA while maintaining high efficiency.

Calculation of load impedance to provide transistor "*soft-switching*"

The voltage at node A (Fig. 1, *b*) is equal to:

$$U(\theta) = \begin{cases} \frac{1}{2}\pi\nu\sin(\nu\theta) - \frac{1}{2}\nu I_0\sin\varphi\sin(\nu\theta) + 1 - \frac{1}{2}\cos(\nu\theta) - \frac{\nu^2 I_0\cos\varphi\cos(\nu\theta)}{4(1-\nu^2)} + \frac{\nu^2 I_0\cos\varphi\cos\theta}{2(1-\nu^2)} - \\ -\frac{I_0\cos\varphi\cos\theta}{4(1-\nu^2)} + \frac{\nu^2 I_0\sin\varphi}{4(1-\nu^2)}\cdot\sin(\nu\theta) + \frac{I_0\sin\varphi\sin\theta}{4(1-\nu^2)} - \frac{\nu^2 I_0\sin\varphi\sin\theta}{2(1-\nu^2)}, \quad 0 < \theta \le \pi; \\ -\frac{1}{2}\pi\nu\sin(\nu\theta) - \frac{1}{2}\nu I_0\sin\varphi\sin(\nu\theta) + \frac{1}{2}\cos(\nu\theta) - \frac{\nu^2 I_0\cos\varphi\cos(\nu\theta)}{4(1-\nu^2)} - \frac{I_0\cos\varphi\cos\theta}{4(1-\nu^2)} + \\ +\frac{\nu^2 I_0\cos\varphi\cos\theta}{2(1-\nu^2)} + \frac{\nu^2 I_0\sin\varphi}{4(1-\nu^2)}\cdot\sin(\nu\theta) + \frac{I_0\sin\varphi\sin\theta}{4(1-\nu^2)} - \frac{\nu^2 I_0\sin\varphi\sin\theta}{2(1-\nu^2)}, \quad \pi < \theta \le 2\pi. \end{cases} \tag{8}$$

In order to compose the harmonic balance equation, the voltage $U(\theta)$ amplitude and phase of the first harmonic are needed:

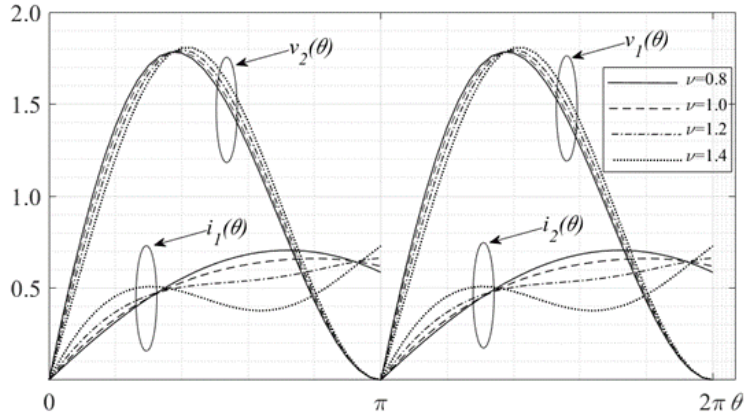

Fig. 2. Time-domain diagrams of the voltage drop and current in transistor at different ν values

$$U_1 = \sqrt{a_1^2 + b_1^2}, \quad \varphi_U = \text{arctg}\frac{b_1}{a_1}, \tag{9}$$

where a_1 and b_1 are the coefficients of the Fourier series:

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} U(\theta)\cos\theta d\theta, \tag{10}$$

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} U(\theta)\sin\theta d\theta. \tag{11}$$

The modulus and phase of the load impedance are equal to:

$$|Z| = \frac{|U_1|}{|I_m|} = \frac{\sqrt{a_1^2 + b_1^2}}{I_m}; \tag{12}$$

$$\varphi_z = \varphi_U - \varphi. \tag{13}$$

Fig. 3 shows the normalized load impedance (real $R_N = ReZ_L / ReZ_0$ and imaginary $X_N = ImZ_L / ReZ_0$ parts) in the frequency band $[f_L, f_U]$ with overlap coefficient $K_\omega = f_L, f_U$, where f_U and f_L are the upper and the lower bounds of the operational frequency band, respectively; ReZ_0 is the real part of load impedance at the upper bound f_U.

The derived dependencies enable parametric synthesis of the load circuit satisfying the required input impedance variation in the frequency band and attenuation above it. Based on the results of solving this synthesis problem it becomes possible to determine the frequency overlap factor K_ω.

Validation of the analytical model

The analytical expressions were validated through a comprehensive simulation using the model shown in Fig. 4, where $S1$, $S2$ – active devices (switches); $V1$ – supply voltage; $V2$, $V3$ – pulse generators; $C1$, $C1$ – capacitances that consider transistors' output ones; $L1$, $L1$ –inductors; Lx, Rl – imaginary and real parts of impedance load, respectively. Fig. 5 plots voltage and current time diagrams.

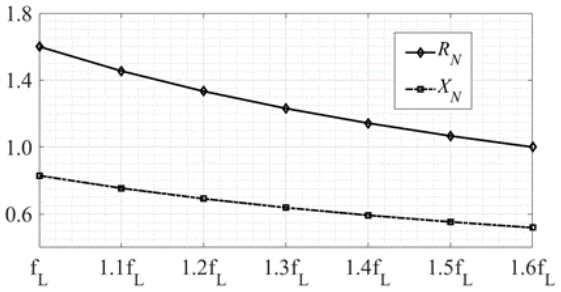

Fig. 3. Normalized impedance load versus frequency

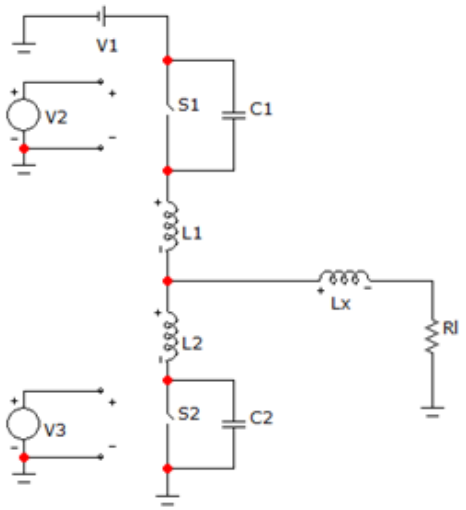

Fig. 4. Class E_V PA simulation model

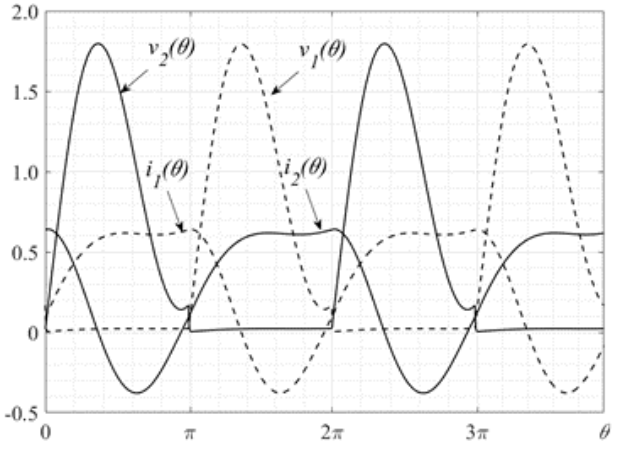

Fig. 5. Simulated curves of voltage and current across switches *S*1, *S*2

Table 2 presents the results obtained using simulation modeling in the frequency band $[fL, f_U]$, where Z_L – normalized complex impedance load; *3f*, *5f* – relative level of 3rd and 5th harmonics; Π – transistors' voltage stress; Δυ – voltage jump on transistors, normalized by supply voltage.

Table 2

Simulation results

F	f_{H}	$1.2f_{\text{H}}$	$1.4f_{\text{H}}$	$1.6f_{\text{H}}$
Z_L	$1.60 + j0.83$	$1.33 + j0.69$	$1.14 + j0.59$	$1.00 + j0.52$
3f, dBc	–24.5	–24.5	–24.5	–24.5
5f, dBc	–40.4	–40.3	–40.4	–40.5
П	1.83	1.82	1.81	1.81
Δυ, %	6.1	6.5	6.4	4.9

As evidenced by the comparative analysis of data in Table 2, the analytical model demonstrates excellent agreement with simulation results, exhibiting: 2.0% relative error in voltage stress (П), 6.5% deviation in voltage jumps (Δυ). However, the harmonic distortion levels remain non-negligible, with the 3rd harmonic at –24 dBc and the 5th harmonic at –40 dBc. This means that the synthesis of the PA filtering and matching circuit must be carried out not only based on the condition of implementing the required law of behavior of the real and imaginary parts of its input impedance, but, in addition to this, considering the required attenuation of a given set of higher harmonics.

Synthesis of a filtering and matching circuit

The requirement to suppress higher harmonics to compliant levels (e.g., < –40 dBc for $n \geq 3$) inherently constrains possible structure options of filtering and matching circuit (FMC) in favor of low-pass filters (LPF) [12, 13]. Taking this constraint into account, the task of FMC synthesis can be formulated as the parametric optimization problem of a number LPF variants of Elliptic and Chebyshev types of diffirent orders. The structures of the Elliptic (E) LPF of the 3rd and 5th orders are shown in Fig. 6, *a*, *b* as well as the Chebyshev LPF of the 5th order is shown in Fig. 7.

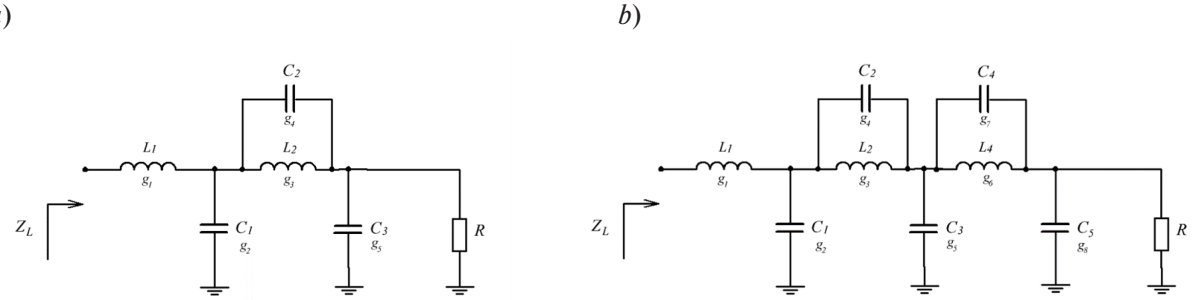

Fig. 6. The structures of 3rd and 5th Order Elliptic LPF

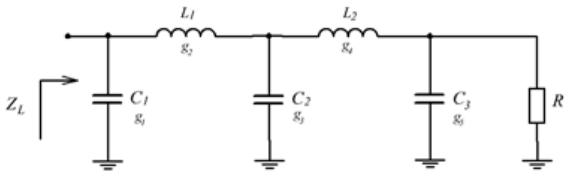

Fig. 7. The structure of 5th Order Chebyshev LPF

The parametric optimization problem can be represented as:

$$\vec{x}^* = \arg\min_{\vec{x}\in D} F\left(\vec{x}, f\right), \tag{14}$$

where $D = \left\{ \begin{array}{c} x_i > 0,\ i = 1 \ldots n \\ \vec{x} \in R^n \left| -2\ dB < 20\log\left|H\left(\vec{x}, f\right)\right| < 2\ dB,\ \text{when}\ f < f_c \right. \\ 20\log\left|H\left(\vec{x}, f\right)\right| \le -40\ dB,\ \text{when}\ f \ge f_s \end{array} \right\}$, $\vec{x}$ is the vector of the LPF elements parameters, f_c is the LPF passband frequency, f_s is the LPF stopband frequency. In this case, the objective function will have the form:

$$F\left(\vec{x}, f\right) = \sum_{k=1}^{m} \sqrt{\frac{\left(ReZ_L\left(f_k\right) - ReZ_F\left(\vec{x}, f_k\right)\right)^2}{ReZ_L\left(f_i\right)^2} + \frac{\left(ImZ_L\left(f_k\right) - ImZ_F\left(\vec{x}, f_k\right)\right)^2}{ImZ_L\left(f_i\right)^2}}, \tag{15}$$

where the set $Z_L(f_k)$ corresponds to the required law of change of the FMC input impedance and $Z_F(f_k)$ – the calculated values of the FMC input within the passband.

The normalized LPF elements values obtained in optimization are given in Table 3, and the load voltage spectrum diagrams are shown in Fig. 8–10.

From the analysis of the diagrams in Fig. 8–10 it follows that the output voltage spectrum contains only odd harmonics, the relative amplitudes of which are given in Tables 4–6. The values of the normalized transistor voltage stress (П) are also presented here. A voltage stress deviation when using different types of LPF from the analytical calculation is shown in Fig. 11.

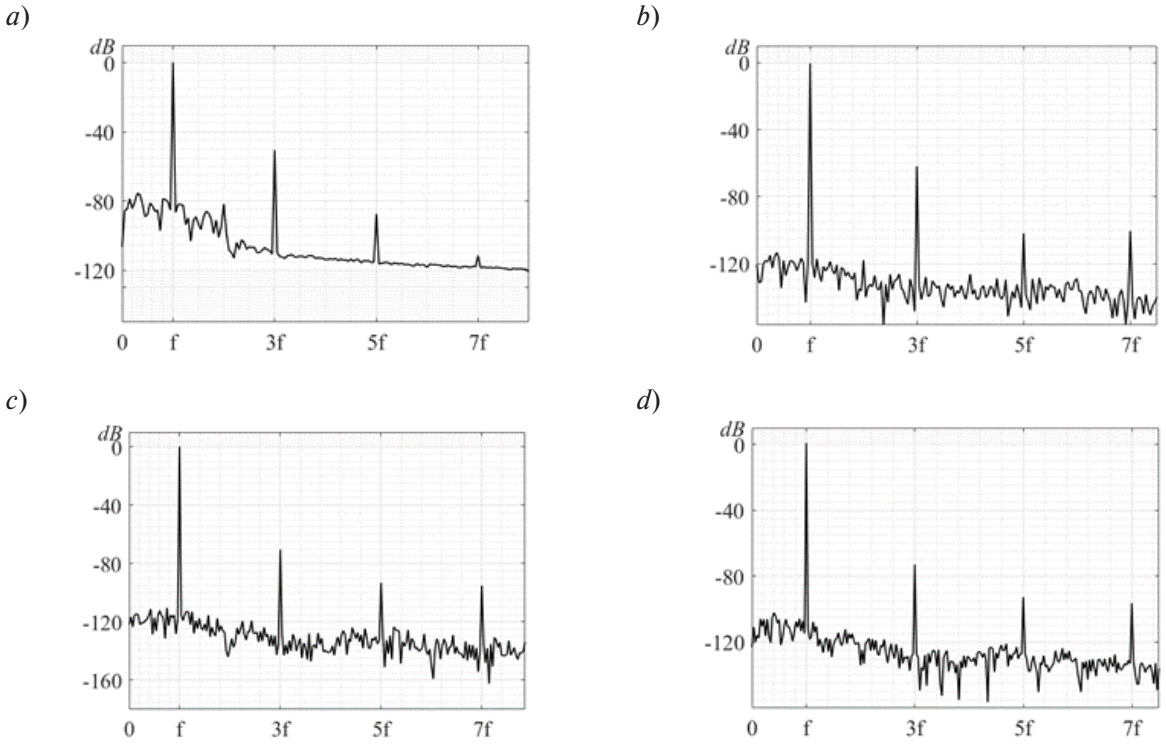

Fig. 8. Load voltage spectrums for a 3rd order elliptic LPF at different operating frequencies: f_L (*a*), $1.2f_L$ (*b*), $1.4f_L$ (*c*), $1.6f_L$ (*d*)

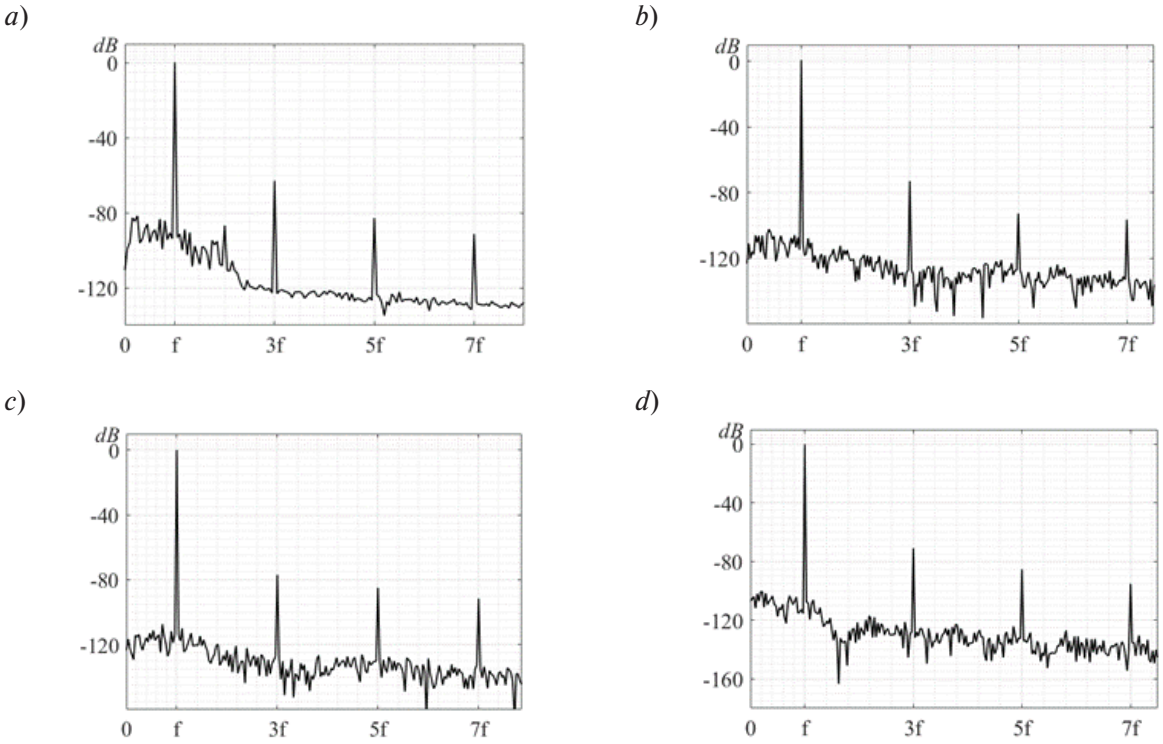

Fig. 9. Load voltage spectrums for a 5th order elliptic LPF
at different operating frequencies: f_L (*a*), $1.2f_L$ (*b*), $1.4f_L$ (*c*), $1.6f_L$ (*d*)

Table 3

Normalized LPF elements values

LPF	Nominal values							
	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8
3rd Order Elliptic	0.704	2.806	1.022	0.061	1.386	–	–	
5th Order Elliptic	0.722	2.734	0.866	0.217	1.039	0.197	1.974	0.489
5th Order Chebyshev	0.051	0.684	2.988	1.034	1.503	–	–	–

Table 4

Characteristics of the PA when implementing FMC on the basis of a 3rd order elliptic LPF

Frequency	Higher-harmonic level, dBc			П
	3	5	7	
f_L	–51	–77	–111	1.92
$1.2f_L$	–54	–91	–100	1.71
$1.4f_L$	–60	–92	–104	1.62
$1.6f_L$	–73	–93	–97	1.86

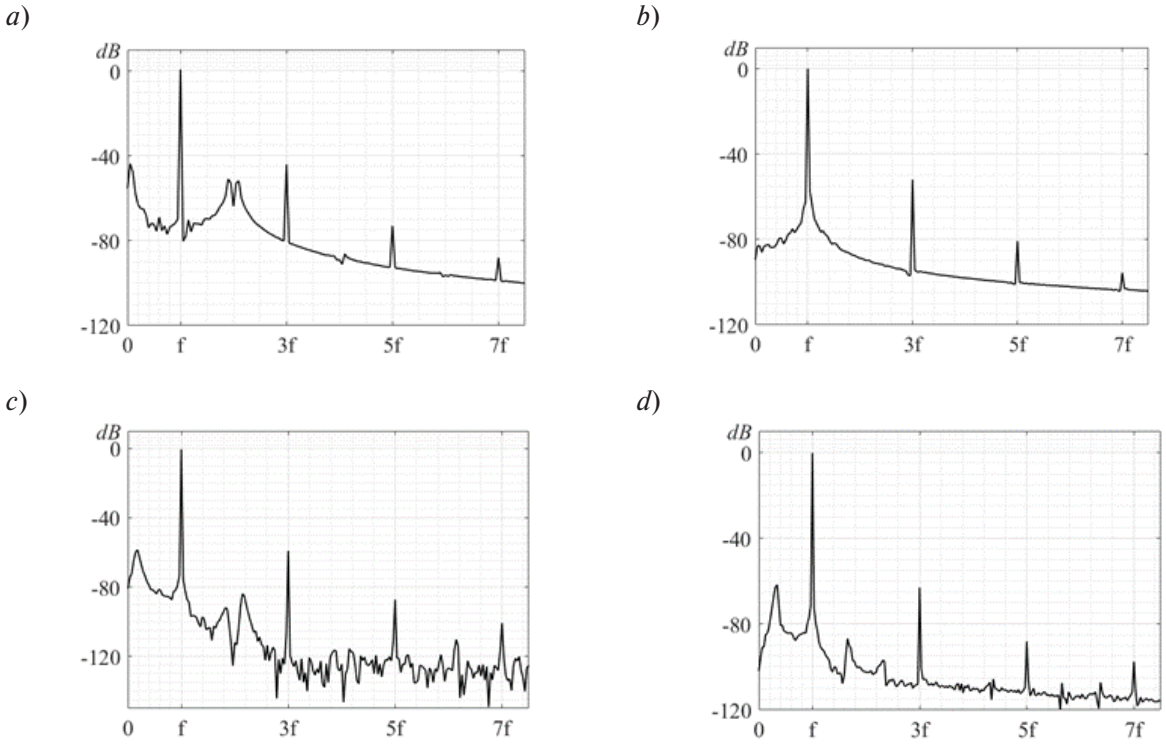

Fig. 10. Load voltage spectrums for a a 5th order Chebyshev LPF at different operating frequencies: f_L (*a*), $1.2f_L$ (*b*), $1.4f_L$ (*c*), $1.6f_L$ (*d*)

A comparative analysis presented in Tables 4–6 and Fig. 11 shows that the FMC based on the 5th order elliptic LPF attenuates higher harmonics better, with the level of the 3rd harmonic being no more than –65 dBc. In the case of 3rd order elliptic LPF, the level of the third harmonic is –51 dBc, and for the 5th order Chebyshev LPF, it is –44 dBc. Using the 5th order elliptic filter also shows results with a smaller theoretical deviation compared to other LPFs. Therefore, it can be concluded that using the 5th order elliptic LPF provides better performance.

Table 5

Characteristics of the PA when implementing FMC on the basis of a 5th order elliptic LPF

Frequency	Higher-harmonic level, dBc			П
	3	5	7	
f_L	–65	–85	–92	1.88
$1.2f_L$	–89	–86	–92	1.74
$1.4f_L$	–73	–84	–90	1.72
$1.6f_L$	–70	–84	–94	1.89

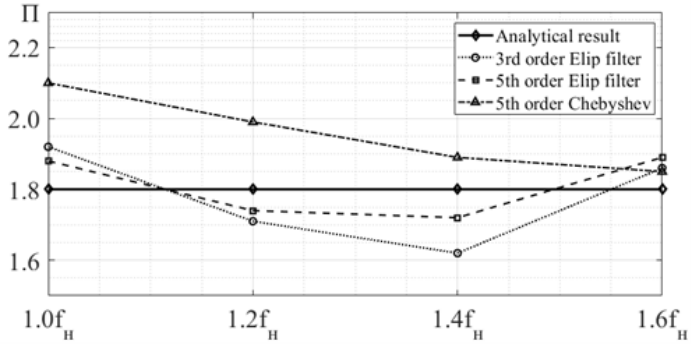

Fig. 11. Comparison of voltage stress deviation when using different types of LPF

Table 6

Characteristics of the PA when implementing FMC on the basis of a 5th order Chebyshev LPF

Frequency	Higher-harmonic level, dBc			П
	3	5	7	
f_L	–44	–72	–87	2.10
$1.2f_L$	–52	–76	–83	1.99
$1.4f_L$	–57	–85	–99	1.89
$1.6f_L$	–63	–88	–97	1.85

Conclusion

Summarizing the results presented in this paper, we highlight the followings:

1) Based on the harmonic balance method, the analytical model of a Class E PA with reduced voltage stress across transistors (Class EV) has been developed which allows for determination of its characteristics when operating a complex impedance load.

2) Using the obtained analytical relations with a known law of load impedance change in the frequency band, the currents and voltages on the elements of the PA can be calculated.

3) The assessment of the adequacy of the proposed analytical model has been carried out which confirmed 2.0% relative error in voltage stress estimation and 6.5% deviation while calculating voltage jump across the transistor at turn-on.

4) A method for synthesizing a filtering and matching circuit is proposed, which allows to expand the operating frequency band of the amplifier with given restrictions on the output power change as well as on the level of switching losses in the transistors, and the permissible level of higher harmonics in the load.

5) The normalized element values of the filtering and matching circuit were optimized, permitting PA operation over a frequency band with an overlap factor of $K_\omega = 1.6$ and decreased switching losses.

6) It has been shown that the relative level of higher harmonics in the output voltage in the case of a 5th-Order Elliptic low-pass filter can be reduce to a value of –65 dB.

REFERENCES

1. **Acar M., Annema A.J., Nauta B.** Analytical design equations for class-E power amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2007, Vol. 54, Pp. 2706–2717. DOI: 10.1109/TCSI.2007.910544

2. **Eroglu A.** *Introduction to RF Power Amplifier Design and Simulation*, 1st ed. Boca Raton: CRC Press, 2016. DOI: 10.1201/9781315215297

3. **Zudov R.I.** Influence of rotational position error stage voltage on the output spectrum in switch power amplifier. *2014 International Conference on Actual Problems of Electron Devices Engineering*, 2014, Pp. 241–243.

4. **Singh G.D., Nallam N.** An RF choke-less Class E power amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020, Vol. 67, No. 11, Pp. 2422–2426. DOI: 10.1109/TCSII.2020.2966552

5. **Yuta I., Hirotaka K.** Choke-less Class -E Oscillator Using p-MOSFET and n-MOSFET. *2023 IEEE 32nd International Symposium on Industrial Electronics* (*ISIE*), June 2023, DOI: 10.1109/ISIE51358.2023.10228146.

6. **Pham H.D., Sorotsky V.A.** Characteristics of Class E power amplifier with complex impedance load. *Computing, Telecommunications and Control*, 2025, Vol. 18, No. 1, Pp. 72–84. DOI: 10.18721/JCSTCS.18106

7. **Sorotsky V., Pham H.D., Zudov R.** Design of a Class E Power amplifier with complex impedance load. *2024 International Conference on Electrical Engineering and Photonics* (*EExPolytech*), 2024, Pp. 76–78. DOI: 10.1109/EExPolytech62224.2024.10755740

8. **Zudov R.** Efficiency of a class DE power amplifier for RF signals with high peak-to-average power ratio. *2019 International Conference on Electrical Engineering and Photonics* (*EExPolytech*), 2024, Pp. 28–30. DOI: 10.1109/EExPolytech.2019.8906856

9. **Grebennikov A.** *RF and Microwave Power Amplifier Design*, 2nd ed. NY: McGraw-Hill, 2015.

10. **Kazimierczuk M.K.** *RF Power Amplifiers*, 2nd ed. Bognor Regis (US): John Wiley & Sons, Ltd, 2015. DOI: 10.1002/9781118844373

11. **Sokal N.O., Grebennikov A.** *Switchmode RF Power Amplifiers*, 1st ed. USA: Elsevier Inc., 2007. DOI: 10.1016/B978-0-7506-7962-6.X5028-X

12. **Chen K., Peroulis D.** Design of highly efficiency broadband class-E power amplifier using synthesized low-pass matching networks. *IEEE Transactions on Microwave Theory and Techniques*, 2011, Vol. 59, No. 12, Pp. 3162–3173. DOI: 10.1109/TMTT.2011.2169080

13. **Kizilbey O.** Design of class-E GaN HEMT power amplifier using elliptic low pass matching network with 86% efficiency. *IEICE Electronics Express*, 2013, Vol. 10, No. 2, Art. no. 20120960. DOI: 10.1587/elex.10.20120960

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