Computing, Telecommunication and Control, 2025, Vol. 18, No. 3, Pp. 123–130.
Информатика, телекоммуникации и управление. 2025. Том 18, № 3. С. 123–130.

Short message
DOI: https://doi.org/10.18721/JCSTCS.18311
UDC 621.3.049.774.2

AN 8-BIT WIDE INPUT SWING ANALOG-TO-DIGITAL CONVERTER BASED ON VOLTAGE-CONTROLLED OSCILLATOR

V.D. Bystrov ✉ , *D.V. Morozov* , *M.M. Pilipko*

Peter the Great St. Petersburg Polytechnic University,
St. Petersburg, Russian Federation

✉ bystrov.vd@edu.spbstu.ru

Abstract. An 8-bit analog-to-digital converter based on a voltage-controlled oscillator using 180 nm CMOS technology from Mikron JSC with a supply voltage of 3.3 V for the analog part and 1.8 V for the digital part is presented. The analog-to-digital converter has a wide range of input voltages from 0 to 3.3 V. The transistor-level simulation of the analog-to-digital converter in the time domain was performed in Cadence Virtuoso. The sampling rate was set to 1 MHz. The power consumption is about 1.8 mW. The dimensions of the designed layout are 103 μm by 109 μm. With an input frequency of 50 kHz and an amplitude of 1.55 V, the post-layout simulation shows an output SNDR of 36.48 dB (ENOB is 5.77 bits).

Keywords: analog-to-digital converter, voltage-controlled oscillator, linearity of the transfer characteristic, digital synthesis

Acknowledgements: The production of the integrated microcircuit was carried out at the expense of the Ministry of Education and Science of Russia within the framework of the federal project “Training of personnel and scientific foundation for the electronic industry” under the state assignment for the implementation of research work “Development of a methodology for prototyping an electronic component base in domestic microelectronic production based on the MPW service”.

Citation: Bystrov V.D., Morozov D.V., Pilipko M.M. An 8-bit wide input swing analog-to-digital converter based on voltage-controlled oscillator. Computing, Telecommunications and Control, 2025, Vol. 18, No. 3, Pp. 123–130. DOI: 10.18721/JCSTCS.18311

Краткое сообщение
DOI: https://doi.org/10.18721/JCSTCS.18311
УДК 621.3.049.774.2

ВОСЬМИРАЗРЯДНЫЙ АЦП С РАСШИРЕННЫМ ДИАПАЗОНОМ ВХОДНОГО СИГНАЛА НА ОСНОВЕ ГУН

В.Д. Быстров ✉ , *Д.В. Морозов* , *М.М. Пилипко*

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

✉ bystrov.vd@edu.spbstu.ru

Аннотация. Представлен восьмиразрядный аналого-цифровой преобразователь на основе генератора, управляемого напряжением, разработанный по 180 нм КМОП-технологии от АО «Микрон» с напряжением питания 3,3 В в аналоговой части и 1,8 В в цифровой части. Аналого-цифровой преобразователь имеет расширенный диапазон напряжений входного сигнала от 0 до 3,3 В. Моделирование преобразователя на транзисторном уровне во временной области проводилось в Cadence Virtuoso. Частота дискретизации была установлена равной 1 МГц. Потребляемая мощность составила около 1,8 мВт. Размеры разработанной топологии кристалла преобразователя составили 103 мкм на 109 мкм. При частоте входного сигнала, равной 50 кГц, и амплитуде 1,55 В, моделирование с учетом экстракции паразитных параметров топологии аналого-цифрового преобразователя показывает на выходе значение отношения сигнала к шуму и искажениям 36,48 дБ (эффективное число бит равно 5,77 бит).

Ключевые слова: аналого-цифровой преобразователь, генератор, управляемый напряжением, линейность передаточной характеристики, цифровой синтез

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научный фундамент для электронной промышленности» по государственному заданию на выполнение опытно-конструкторской работы «Разработка методики прототипирования элементной базы электроники на отечественных микроэлектронных производствах на основе сервиса MPW».

Для цитирования: Bystrov V.D., Morozov D.V., Pilipko M.M. An 8-bit wide input swing analog-to-digital converter based on voltage-controlled oscillator // Computing, Telecommunications and Control. 2025. Т. 18, № 3. С. 123–130. DOI: 10.18721/JCSTCS.18311

Introduction

The trend towards an increase in the number of sensors in areas such as the IoT, medical care and mechanical engineering has led to an increased need to use many analog-to-digital converters (ADCs). Since many devices are autonomous, ADCs must provide low power consumption [1–4]. Also, with the scaling of CMOS technology, there is a tendency to transfer the signal processing complexity to the digital domain [5]. The mentioned trends are supported by an ADC based on a volt age-controlled oscillator (VCO). The VCO-based ADC block diagram is shown in Fig. 1 (DU stands for digital unit). The analog signal is sent to the VCO input. A VCO converts the input signal level into the frequency of the output pulses. The digital unit counts the number of pulses per sampling cycle and generates the corresponding binary code at the output. The typical values of the bit depth of the ADC type in question depend on the technology used. For technologies larger than 100 nm, bit depths of up to 10 bits are more common [6, 7]. In cases of implementation using technology less than 100 nm, a bit depth of 15 bits is often found [8–10].

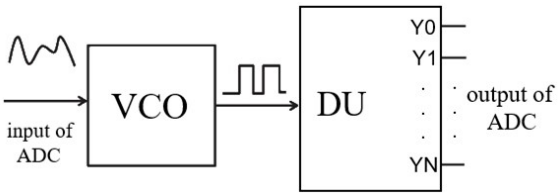


Fig. 1. Block diagram of an ADC based on a VCO

Circuit of the VCO

Fig. 2 shows the developed circuit of the VCO in complementary metal-oxide-semiconductor (CMOS) technology. The VCO core is three inverters connected in a ring. These inverters are formed by transistors M1–M6. Also, an output inverter on transistors M17 and M18 is connected to the output of one of the inverters to reduce the rise and fall time of the output pulse signal of the VCO. Limiting transistors M10–M12 and M14–M16 are used to control the frequency of VCO. These transistors limit the current consumed by the VCO core inverters during operation. The lower the maximum current through the limiting transistors, the more time the inverter needs to recharge the parasitic capacity of the next inverter, therefore, the lower the frequency of pulses. With the help of current mirrors formed by transistors M8, M9, M13–M16, the maximum current through the limiting transistors is set. The control current is formed by a voltage converter into a current formed by the transistor M7 and resistors R_1, R_2, R_h, R_s. The linearity of the VCO transfer characteristic is provided by the linear transfer characteristic of the voltage-to-current converter [11]. Resistors R_1, R_2, R_s provide an extension of the linearity range of the transfer characteristic. The resistor R_h is used to adjust the VCO gain [12]. By independently changing the channel width of the limiting transistors, the channel width of the transistor M7, and the values of the resistors R_h, R_s, it is possible to set the required maximum and minimum pulse generation frequency of the VCO.

Design of the ADC digital unit

The digital unit of the proposed ADC consists of a subtracting counter and a parallel register. The counter counts the number of pulses received at its input during the sampling period. The counter's bit depth is equal to the ADC's bit depth, in our case, it is 8 bits. The register is necessary to fix the counter value according to the sampling cycle. To design the digital unit of the ADC, automatic synthesis of digital circuits from the hardware description was applied. The hardware descriptions of the counter, the parallel register, and the ADC digital unit are shown in Listings 1–3, respectively.

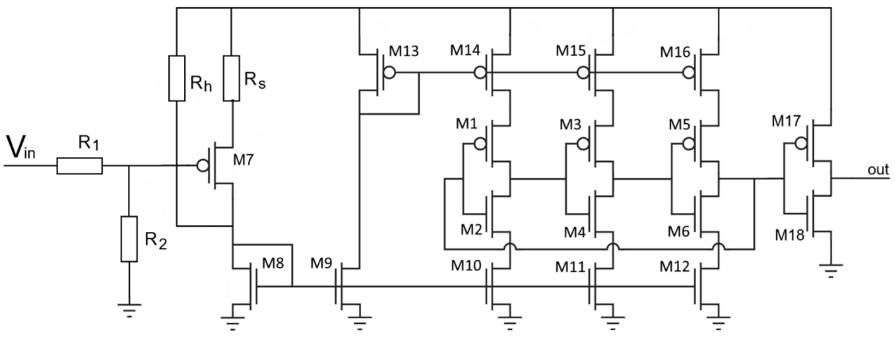


Fig. 2. Circuit of the VCO

Listing 1. Hardware description of the counter

```
module sabstrcnt(r, c, x, y);

	input r, c, x;
	output reg [7:0]y;
	always @( negedge r, posedge x, posedge c)
	begin
		if(!r)
			y <= 'd255;
		else
		begin
			if (c)
				y <= 'd255;
			else
				y <= y-'d1;
		end
	end

endmodule
```

Listing 2. Hardware description of the parallel register

```
module parr(r,c,x,y);

	input r, c;
	input [7:0]x;
	output reg [7:0]y;
	always @( negedge r, posedge c)
		if (!r)
			y <= 0;
		else
			y <= x;

endmodule
```

Listing 3. Hardware description of the ADC digital unit

```
module DU(r,c,x,y);

	input r,c,x;
	wire [7:0]w;
	output [7:0]y;

	sabstrcnt A(r,c,x,w);
	parr B(r,c,w,y);

endmodule
```

The digital unit of the ADC was synthesized using the built-in CAD tools. The circuit was synthesized from standard cells using 180 nm CMOS technology with a supply voltage of 1.8 V from Mikron JSC. The circuit of the digital unit is shown in Fig. 3.

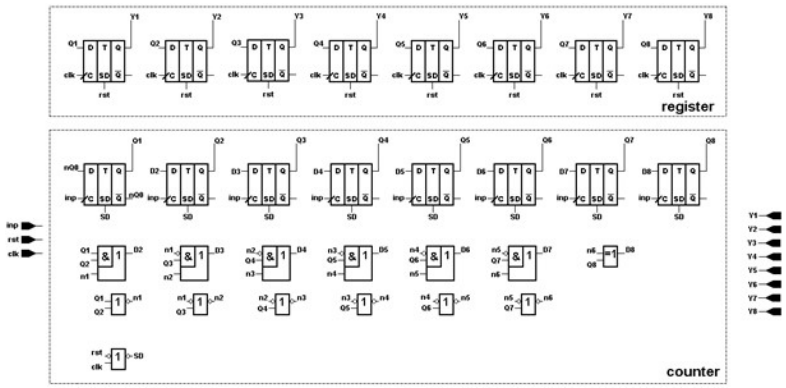


Fig. 3. Circuit of the digital unit of the ADC

Layout of the ADC

Fig. 4 shows the layout of the designed ADC based on the VCO. The VCO is located in the upper left part of the layout. To the right of the VCO, three inverters connected in series are placed. These three inverters convert the amplitude of the VCO output pulses from 3.3 to 1.8 V, because the digital unit of the ADC is designed using cells with a supply voltage of 1.8 V.

The quantization error of the VCO-based ADC depends on the difference between the rise and fall times of the pulse, herewith it is minimal if the difference is zero [13]. The digital unit of the ADC is located at the bottom of the layout in Fig. 4. The D flip-flop cells of the counter are located closest to the VCO, while the combinational logic is located below them. The D flip-flop cells of the output register are located on the right and bottom sides of the layout of the ADC digital unit. The dimensions of the ADC layout are 103 μm by 109 μm.

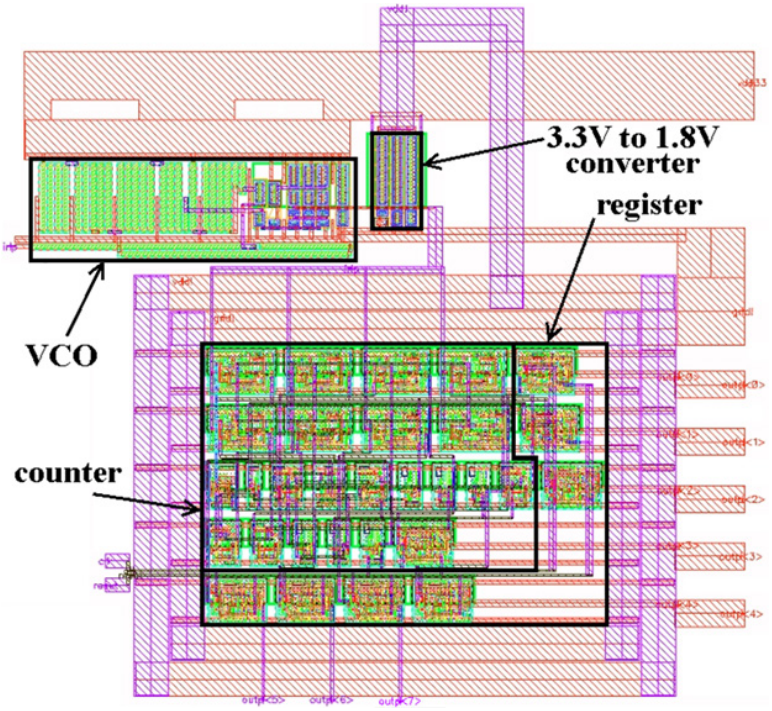
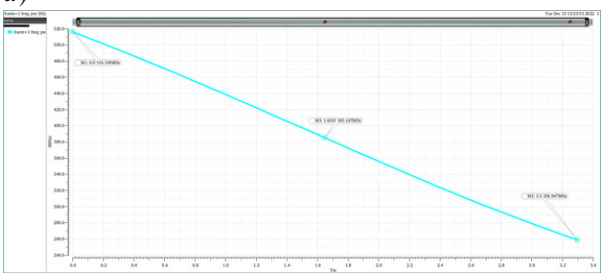


Fig. 4. VCO-based ADC layout

a)



b)

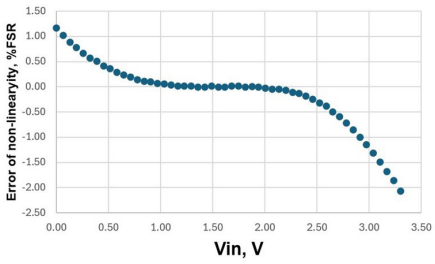


Fig. 5. Simulation of the transfer characteristic of the VCO

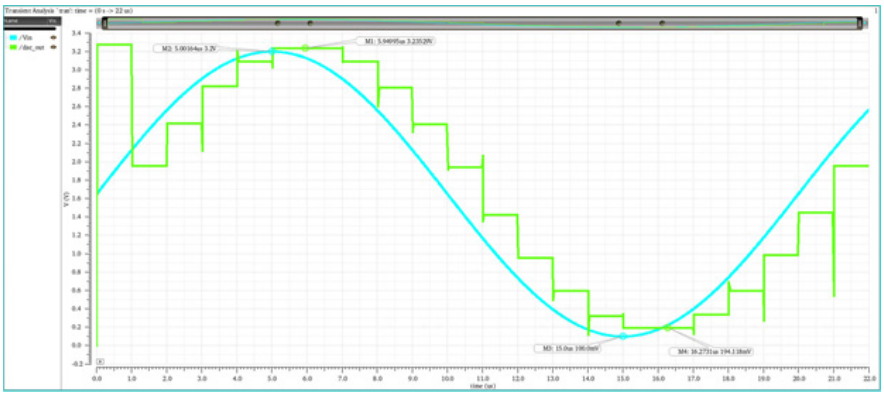


Fig. 6. ADC input and output signals

Simulation of ADC operation

A simulation of the operation of the VCO-based ADC was carried out. Since the characteristics of the ADC depend on the linearity of the transfer characteristic of the VCO, the dependence of the frequency of VCO on the input signal level was built. Fig. 5a shows the transfer characteristic of the VCO obtained using the PSS analysis. Fig. 5b shows a graph of the dependence of the nonlinearity error on the ADC input signal level. The average error of the nonlinearity of the VCO gain is 0.43% of the full scale of measurements (FSR).

Fig. 6 shows the input and output signals of a VCO-based ADC. The amplitude of the input signal was set to 1.55 V, and the frequency was 50 kHz. The outlier in the output signal of the ADC at the initial time occurred due to the initial values in the output register. Using the built-in Cadence Virtuoso tools, the ADC dynamic characteristics were determined based on the output signal spectrum. The values for the first sampling cycle of the ADC output signal were not used when calculating the parameters. A signal-to-noise ratio (SNDR) of 36.48 dB has been achieved which means an effective number of bits (ENOB) of 5.77 bits.

Conclusion

An 8-bit voltage-controlled oscillator-based ADC with a range of input values from 0 to 3.3 V using 180 nm CMOS technology from Mikron JSC with a supply voltage of 3.3 V in the analog part and 1.8 V in the digital part is presented. The simulation of the ADC in the time domain was performed in Cadence Virtuoso. The sampling rate was set to 1 MHz. The power consumption is about 1.8 mW. With an input frequency of 50 kHz and an amplitude of 1.55 V, the ADC provides an output SNDR of 36.48 dB (ENOB is 5.77 bits). This low-power design is applicable in the IoT, medical care and other autonomous devices.

REFERENCES

1. **Gielen G.G.E., Hernandez L., Rombouts P.** Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital CMOS-part 1: Basic principles. *IEEE Solid-State Circuits Magazine*, 2020, Vol. 12, No. 2, Pp. 47–55. DOI: 10.1109/MSSC.2020.2987536

2. **Li S., Sanyal A., Lee K., Yoon Y., Tang X., Zhong Y., Ragab K, Sun N.** Advances in voltage-controlled-oscillator-based δσ ADCs. *IEICE Transactions on Electronics*, 2019, Vol. 102, No. 7, Pp. 509–519. DOI: 10.1587/transele.2018CTI0001

3. **Anand T., Makinwa K.A.A., Hanumolu P.K.** A VCO based highly digital temperature sensor with 0.034 C/mV supply sensitivity. *IEEE Journal of Solid-State Circuits*, 2016, Vol. 51, No. 11, Pp. 2651–2663. DOI: 10.1109/JSSC.2016.2598765

4. **Tu C.-C., Wang Y.-K., Lin T.-H.** A low-noise area-efficient chopped VCO-based CTDSM for sensor applications in 40-nm CMOS. *IEEE Journal of Solid-State Circuits*, 2017, Vol. 52, No. 10, Pp. 2523–2532. DOI: 10.1109/JSSC.2017.2724025

5. **De la Rosa J.M., Schreier R., Pun K.-P., Pavan S.** Next-Generation delta-sigma converters: Trends and perspectives. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2015, Vol. 5, No. 4, Pp. 484–499. DOI: 10.1109/JETCAS.2015.2502164

6. **Quintero A., Buffa C., Perez C., Cardes F., Straeussnigg D., Wiesbauer A., Hernandez L.** A coarse-fine VCO-ADC for MEMS microphones with sampling synchronization by data scrambling. *IEEE Solid-State Circuits Letters*, 2020, Vol. 3, Pp. 29–32. DOI: 10.1109/LSSC.2020.2964158

7. **Ellaithy D.M.** Voltage-controlled oscillator based analog-to-digital converter in 130-nm CMOS for biomedical applications. *Journal of Electrical Systems and Information Technology*, 2023, Vol. 10, Art. no. 38. DOI: 10.1186/s43067-023-00109-x

8. **Shibata H., Taylor G., Schell B., Kozlov V., Patil S., Paterson D. et al.** 16.6 an 800MHz-BW VCO-based continuous-time pipelined ADC with inherent anti-aliasing and on-chip digital reconstruction filter. *2020 IEEE International Solid-State Circuits Conference* (*ISSCC*), 2020, Pp. 260–262. DOI: 10.1109/ISSCC19947.2020.9062917

9. **Wu T.-F., Chen M.S.-W.** 16.7 A 40MHz-BW 76.2dB/78.0dB SNDR/DR noise-shaping nonuniform sampling ADC with single phase-domain level crossing and embedded nonuniform digital signal processor in 28nm CMOS. *2020 IEEE International Solid-State Circuits Conference* (*ISSCC*), 2020, Pp. 262–264. DOI: 10.1109/ISSCC19947.2020.9063022

10. **Zhong Y., Li S., Tang X., Shen L., Zhao W., Wu S., Sun N.** A second-order purely VCO-based CT ΔΣ ADC using a modified DPLL structure in 40-nm CMOS. *IEEE International Solid-State Circuits*, 2020, Vol. 55, No. 2, Pp. 356–368. DOI: 10.1109/JSSC.2019.2948008

11. **Andryzcik S., Graham D.W.** Linearization of voltage-controlled oscillators using floating-gate transistors. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021, Vol. 68, No. 7, Pp. 2337–2341. DOI: 10.1109/TCSII.2021.3059109

12. **Voelker M., Pashmineh S., Hauer J., Ortmanns M.** Current feedback linearization applied to oscillator based ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2014, Vol. 61, No. 11, Pp. 3066–3074. DOI: 10.1109/TCSI.2014.2327302

13. **Razavi B.** *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*. Cambridge (UK): University Printing House, 2020. DOI: 10.1017/9781108626200

INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Vitaly D. Bystrov
Быстров Виталий Дмитриевич
E-mail: bystrov.vd@edu.spbstu.ru

Dmitry V. Morozov
Морозов Дмитрий Валерьевич
E-mail: dvmorozov@inbox.ru
ORCID: https://orcid.org/0000-0003-3403-0120

Mikhail M. Pilipko
Пилипко Михаил Михайлович
E-mail: m_m_pilipko@rambler.ru
ORCID: https://orcid.org/0000-0003-3813-6846

Submitted: 20.05.2025; Approved: 12.09.2025; Accepted: 22.09.2025.
Поступила: 20.05.2025; Одобрена: 12.09.2025; Принята: 22.09.2025.