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STABILIZED REFERENCE CURRENT SOURCE FOR BIOMEDICAL APPLICATIONS

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Abstract. Neurostimulators are devices used to electrically stimulate the nervous system. They are a promising alternative to existing pharmacological methods of treating neurological disorders. The paper presents the current driver, one of the key blocks for providing electrical stimulation. The basic requirements and characteristics of this device are described. The noise of the reference current source, current mirror has been analyzed and the effect of the differential amplifier noise on the total noise current at the output devices has been considered. Based on the results of the analysis, a method for estimating the required output impedance of the current driver is proposed. The circuit implemented in 180 nm CMOS process. The output impedance of not less than 30 MOhm is obtained at the output current of 140 μA and the voltage compliance of 90.9% of the supply voltage. A comparative analysis of the results with the work of other authors is given.

Keywords: current source, neurostimulation, noise PSD, output impedance, feedback

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СТАБИЛИЗИРОВАННЫЙ ИСТОЧНИК ТОКА ДЛЯ БИОМЕДИЦИНСКИХ ПРИМЕНЕНИЙ

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Аннотация. Нейростимуляторы являются многообещающей альтернативой существующим фармацевтическим методам при лечении широкого спектра неврологических заболеваний. В работе рассмотрена реализация драйвера тока, применяемого в нейростимуляторах. Описаны основные требования и характеристики данного устройства. Предложен алгоритм расчета минимально необходимого выходного сопротивления, построенный на основе анализа шума схемы источника опорного тока. Результаты подтверждены моделированием с использованием отечественной КМОП технологии с разрешением 180 нм. Получено выходное сопротивление не менее 30 МОм при выходном токе 140 мкА и диапазоне рабочих напряжений 90,9% от напряжения питания. Приведен сравнительный анализ результатов с работами других авторов.

Ключевые слова: источник тока, нейростимуляция, спектральная плотность мощности шума, выходное сопротивление, обратная связь

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию на выполнение научно-исследовательской работы «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW».

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Introduction

Neurological disorders, such as chronic pain, Parkinson's disease, Alzheimer's disease, Huntington's disease, epilepsy, obesity and addiction, affect a large part of the world's population. The effectiveness of currently available pharmaceutical therapies is limited, because patients become resistant to treatment with long-term use. In addition, these treatments often have unwanted side effects. An alternative treatment option is neurostimulation – changing the properties of nerve tissue through the targeted application of electrical current. The challenge is to develop neurostimulators that meet safety, energy efficiency and performance requirements.

Patient safety requires the use of current-controlled differential stimulation, in which a certain amount of charge is injected into the nerve tissue during the positive phase and is pumped out during the negative phase. One of the main safety requirements is the reduction of the residual charge, as it can cause damage to the nerve tissue or premature fibrotic tissue formation and a decrease in the patient's response. The shape of the current pulses is usually rectangular, but there are studies suggesting that pulses with complex shapes may be safer [1]. On the other hand, it is possible to generate pulses with complex shapes using a current-steering digital-to-analog converter (DAC) with appropriate control signals.

The current driver is the block that stabilizes the stimulation current amplitude and, optionally, adjusts the current amplitude. In essence, it acts as a complex current source and should therefore have the same basic requirement of high output impedance. Nevertheless, this parameter is not sufficient, and another one should be added according to the specificity of the application – the dynamic range of the output voltage or, as it is often called, the compliance voltage. The nature of this parameter is as follows. The stimulation electrodes are connected between the driver and the supply or ground level (depending on whether nMOS or pMOS current mirror is used), so the voltage drop across the electrodes should be as high as possible [1]. It can also be described as the maximum load and electrode equivalent resistance at the maximum output current, according to Ohm's law. At the lower output currents, the compliance voltage is higher due to the lower MOSFET overdrive voltage at the lower currents.

Any work devoted to the design of a stimulation unit for a neurostimulator is aimed at ensuring patient safety. Therefore, the highest possible output impedance of the stimulating unit needs to be achieved to ensure proper operation under different conditions and electrode types.

One of the traditional approaches to enhancing the output impedance of a current mirror involves extending the channel length of the current-sourcing (or current-sinking, in nMOS configurations) transistor. While this technique allows measurable improvements in output impedance, the improvement is relatively modest compared to the substantial area overhead incurred, making it unsuitable for use in implantable applications. The second method is to apply circuit techniques to stabilize the output current. One of the most obvious techniques is cascoding, in which the output impedance is proportional to the common base transistor's intrinsic gain. Although it is possible to achieve output impedances of up to 100 MΩ, there is a problem of high voltage drop across the current mirror, as discussed in [3]. A more interesting approach is to use voltage stabilization circuits based on differential or instrumental amplifiers (Op-Amp), as implemented in [1–2, 4–7]. This allows the operating point of the current sourcing transistor to be stabilized so that any variations in the output voltage are compensated by the stabilization circuit.

In addition, there is no restriction on the current sourcing transistor being in the active region, in fact the triode region can also be used to achieve higher voltage compensation. Finally, all the output impedance boosting techniques discussed can be combined. For example, in [5], an increasing channel length of transistors (up to 1um) is used and a complex stabilization circuit consisting of two 70 dB Op-Amps. The result is an output impedance of 320 GΩ. However, no one mentions the upper and lower limits on the amount of the output impedance. The lower limit should obviously be specified in the medical requirements for the device. However, a review of the literature did not reveal specific values, possibly because quantitative studies of the effect of residual charge on nerve tissue damage have not been published. In this regard, it was decided to find the output impedance limitation from above, i.e., the maximum possible current stability that we can provide with a typical circuit.

Output impedance impact on current stability

In simple terms, the stimulation process involves pumping charge into neural tissue and then compensating for the pumped charge (i.e., pumping charge in the opposite direction).

The impedance of the electrode/neural tissue interface acts as the load impedance and, to a first-order approximation, can be represented as a resistor (including the electrode and electrolyte resistances) and capacitor (including the electrode capacitance and the double layer capacitance) in series (R_L and C_L, respectively).

In deep brain stimulation (DBS) applications, maintaining precise current delivery is crucial for both therapeutic efficacy and patient safety. The load resistance in such systems typically varies between 1 and 10 kΩ [8], with these fluctuations potentially affecting both current stability and charge balance during stimulation. Understanding the nature of these impedance changes is essential for designing robust DBS systems.

Load impedance variations in DBS can be categorized into two types based on their temporal characteristics. The first are long-term impedance changes, which may be caused by formation of fibrous tissue encapsulation around implanted electrodes (a natural biological response) or by using different electrode materials or designs with varying intrinsic impedance characteristics. These occurs over several weeks or months after implantation and change slowly relative to stimulation pulse durations (typically 1 to 100 ms). Therefore, it has minimal effect on instantaneous charge balance during individual pulses, but periodic system recalibration may be required, which, however, does not significantly contribute to excess charge accumulation.

The second category includes short-term impedance fluctuations caused by dynamic polarization of neural tissue during current flow [9] or by asymmetric charge/discharge behavior of the electrode-tissue interface (modeled as a double-layer capacitor). Such fluctuations occur within each stimulation pulse phase and exhibit rapid changes on millisecond timescales. Thus, it significantly affects instantaneous current delivery and can lead to substantial charge imbalance, if not properly compensated.

The stability of the output current in the face of load variations is fundamentally determined by the output impedance $\left(R_{out}\right)$ of the current source. The relationship between load variation $\left(\Delta R_L\right)$ and resulting current variation $\left(\Delta I_{R_L}\right)$ can be analyzed using current divider principles:

$$\Delta I_{R_L} = I_{strim} \cdot \frac{\Delta R_L}{R_{out} + \Delta R_L + R_L}, \tag{1}$$

where I_{strim} is the nominal stimulation current, R_L is the baseline load resistance, ΔR_L is the impedance variation. The trade-off in implementation is that higher output impedance improves current regulation, but may compromise power efficiency. Circuit techniques like active feedback can achieve high R_{out} without excessive output voltage drop.

Enhanced current stabilization using Op-Amps in feedback circuits

One of the most effective techniques for stabilizing current in modern analog circuits involves integrating Op-Amps within a feedback loop to precisely regulate the operating points of current mirror transistors. This paper focuses on the regulated drain current mirror (RDCM) due to its superior performance in maintaining consistent output current. The output impedance of this configuration can be derived using the following equation:

$$Z_{out} \approx A \cdot g_m \cdot r_o^2, \tag{2}$$

where A is the open-loop gain of the Op-Amp, g_m is the transconductance of the MOSFET, r_o is the intrinsic output impedance of the transistor. To achieve an ultra-high output impedance exceeding 100 GΩ, the Op-Amp must provide a gain of at least 70 dB, as per the given expression. However, while the equation suggests no strict upper limit on impedance, practical constraints arise from thermal and flicker noise, which ultimately determine the maximum achievable performance.

Noise analysis and optimization strategies

The intrinsic noise of the circuit significantly impacts the stability of the output current. To assess this, the power spectral density (PSD) of the noise at the driver's output was analyzed, considering contributions from: the reference current source, the current mirror transistors, the Op-Amp.

The RDCM amplifies the reference current by a factor K, a common approach to maintaining current accuracy while minimizing power dissipation and chip area. The total output noise PSD $\left(S_{i_{out}}\right)$ is expressed as:

$$S_{i_{out}} = S_{i_{drv}} + K^2 \cdot S_{i_{ref}}, \tag{3}$$

when $K > 1$, the reference current noise becomes the dominant contributor. Using the SPICE LEVEL 2 MOSFET model, the noise PSD can be broken down into thermal and flicker noise components:

$$S_i = \frac{g_m^2 K_F}{L \cdot W \cdot C_{ox}} \cdot \frac{1}{f} + 4 \cdot k_B \cdot T \cdot \left(g_{mb} + \frac{2}{3} g_m \right), \tag{4}$$

where K_F is the flicker noise coefficient, C_{ox} is the gate oxide capacitance, f is the frequency, W and L are the transistor dimensions, k_B is the Boltzmann constant, T is the absolute temperature, g_{mb} accounts for substrate bias effects.

Since flicker noise ($1/f$ noise) dominates in low-frequency applications, its reduction is critical. Equation (4) reveals that flicker noise is inversely proportional to the transistor area ($W \times L$). Therefore, one of the key strategies that can be employed is increasing transistor dimensions. Using larger MOSFETs in the reference current source reduces flicker noise, but requires careful layout optimization to avoid excessive parasitic capacitance. By implementing this method, a lower noise floor can be achieved, enabling higher output impedance without compromising.

Analysis of noise compensation in feedback circuit

The differential amplifier is used to stabilize the voltage at the drain of the current sourcing transistor M44 in Fig. 1. The common mode voltage at the drain of transistor M44 or at the input of the Op-Amp is lower than the threshold voltage. Therefore, a folded cascode circuit of the Op-Amp is used. Let us consider the feedback analysis to show the effect of the Op-Amp noise on the output noise level of the proposed circuit. For this purpose, let us make a structural diagram of the stabilization circuit and its graph as shown in Fig. 2, *b* and *c*, respectively.

The expression for the transfer function of the Op-Amp noise and for the noise of the reference current source are obtained using Mason's formula.

$$T_{n_{OA}}(p) = \frac{T_{GS}(p)}{1 + T_{OA}(p) \cdot T_{GS}(p)} = \frac{1}{T_{OA}(p) + \frac{1}{T_{GS}(p)}}; \tag{5}$$

$$T_{n_{ref}}(p) = \frac{T_{OA}(p) \cdot T_{GS}(p)}{1 + T_{OA}(p) \cdot T_{GS}(p)} = \frac{1}{1 + \frac{1}{T_{OA}(p) \cdot T_{GS}(p)}}, \tag{6}$$

where $T_{GS}(p)$, $T_{OA}(p)$ are the transfer functions respects to the directed graph in the Fig. 2. In precision analog circuits, single-pole transfer functions are often employed to model system behavior. The DC transfer function of the transconductance stage ($T_{GS}(p)$) approximates unity, while the Op-Amp exhibits a DC gain typically exceeding 100. As a result, equation (5) demonstrates that the intrinsic noise of the Op-Amp is effectively suppressed within the closed-loop bandwidth of the control system. Consequently, its impact on the output noise current becomes negligible under normal operating conditions.

However, equation (6) reveals a critical limitation: the reference current source introduces noise components that appear unattenuated in the output current path. Consequently, this noise contribution becomes the primary limiting factor for the circuit's total noise characteristics.

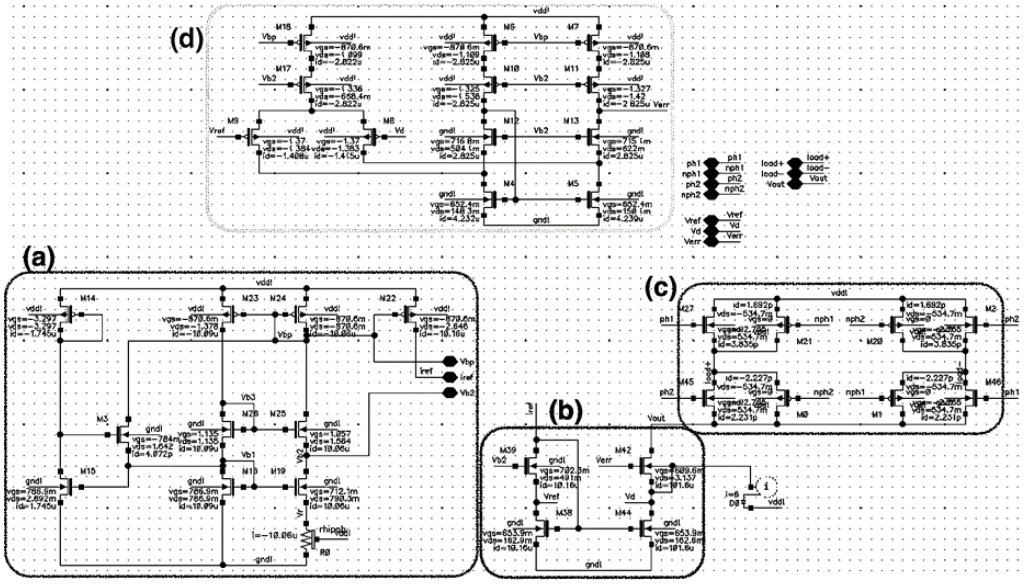

Fig. 1. Proposed reference current source circuit: start-up circuit (*a*), current driver (*b*), bipolar pulse forming circuit (*c*), Op-Amp (*d*)

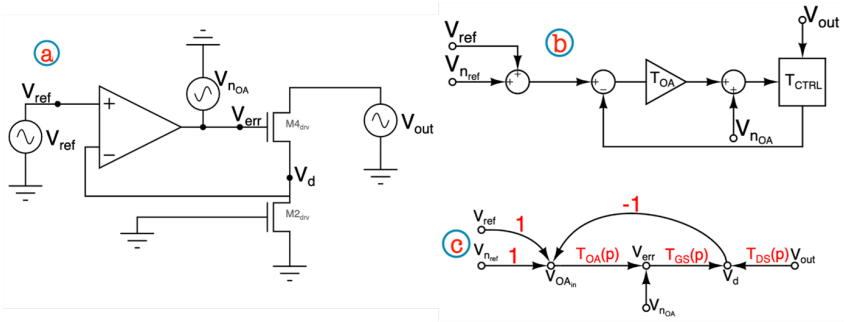

Fig. 2. Stabilizer circuit schematic (*a*), diagram (*b*) and graph (*c*)

In an ideal (noiseless) scenario, the voltage at node V_d (Fig. 2) is stabilized with an accuracy inversely proportional to the Op-Amp's gain. Thus, increasing the gain enhances output current stability, but only up to a certain point. Beyond this, circuit noise – primarily from the reference current source and thermal effects imposes a fundamental limit on stabilization precision.

Additionally, the frequency response of the Op-Amp plays a crucial role. Excessive bandwidth increases high-frequency noise, degrading signal integrity. Insufficient bandwidth restricts the circuit's ability to track and regulate current at the desired frequencies. Therefore, optimal Op-Amp design requires a careful balance: moderate gain selection (high enough to ensure stability, but not so high that noise dominates) and controlled bandwidth (wide enough to meet frequency requirements, but narrow enough to minimize noise amplification). By carefully considering these trade-offs, highly stable current outputs while minimizing noise-induced errors can be achieved.

Proposed estimation algorithm

The output current variations caused by the load impedance variations depend on the driver output impedance and are determined by the current divider formula (1). In turn, the noise-induced variations can be defined as the RMS noise current at the output of the circuit. Equating these two quantities gives the expression:

$$\Delta I_{R_L} = I_{n_{rms}} = \frac{\Delta R_L}{R_L + R_{out_{\max}}} \cdot I_{out}. \quad (7)$$

Expressing the output impedance from expression (7), we obtain the value of the feasible output impedance. As a good approximation, we can assume that the value of the load impedance varies from its typical value R_L to 0. In other words, assuming $\Delta R_L = R_L$ and that the output current is much larger than the RMS noise current, we obtain the following expression:

$$R_{out_{\max}} = \frac{I_{out}}{I_{n_{rms}}} \cdot \Delta R_L - R_L \approx \frac{I_{out}}{I_{n_{rms}}} \cdot R_L. \quad (8)$$

This formula can be used to estimate the required current driver output impedance for the given noise level at the driver output.

Design considerations using proposed estimation algorithm

The current driver designed in 180 nm process, using a 3.3 V supply voltage to ensure sufficient voltage headroom for driving high-impedance loads. This voltage selection was critical to maximize the achievable load resistance range and provide sufficient overdrive voltage for proper transistor operation.

As the reference current source constitutes the primary noise contributor in the system, our design methodology prioritized its optimization through: flicker noise reduction (which includes implementing large-area transistors, using pMOS devices for the reference branch, due to their superior flicker noise characteristics, and applying layout techniques, such as common-centroid placement, to reduce process variations) and architecture selection (adopted an Op-Amp-free architecture of the reference current source to reduce power consumption, minimize additional noise sources simplify circuit in micron process).

Therefore, a modified beta-multiplier reference with additional current mirroring transistors (M25, M26) have been implemented to improve output impedance, enhance power supply rejection and set operating points of the amplifier.

Simulation of a Current Driver in 180 nm CMOS Technology

Fig. 1, *a*, shows the schematic of the proposed reference current source. A parametric analysis was considered to make a trade-off between noise level and IC area. A transistor channel length of 3 μm was used. The transistor widths were chosen to give a nominal current of 10 μA.

This results in a noise RMS current of 3.4 nA. At start-up, the reference current source has two possible states: normal operation and zero current operation, like any self-biased circuit. To ensure normal operation, the start-up circuit shown in Fig. 1, *a* was added, consisting of transistors M14, M15 and M3. Fig. 3 shows the operation of the circuit on power-up without the start-up circuit (top diagram) and with the start-up circuit (bottom diagram).

The RMS value of the noise current can be used to evaluate the required output impedance using equation (8), and consequently the required gain of the differential amplifier using equation (2). The spectral density of the noise current at the output of the reference source is 3.4 nA for the circuit shown in Fig. 1, *a*. Considering that the current mirror has a gain factor $K = 10$, the RMS noise current at the output is more than 34 nA. The required output impedance according to (7) is roughly 30 MΩ. Taking into account the small signal parameters of the MOS transistor typical for 180 nm CMOS technology, we obtain the required gain of 56 dB. A folded cascode Op-Amp is used because the common mode voltage (V_{CM}) at the input of the Op-Amp is about 163 mV, well below the threshold voltage (V_{th}).

The DC analysis of the driver circuit reveals several interesting characteristics that validate the design approach. Fig. 4 shows the key performance metrics, presenting the output impedance

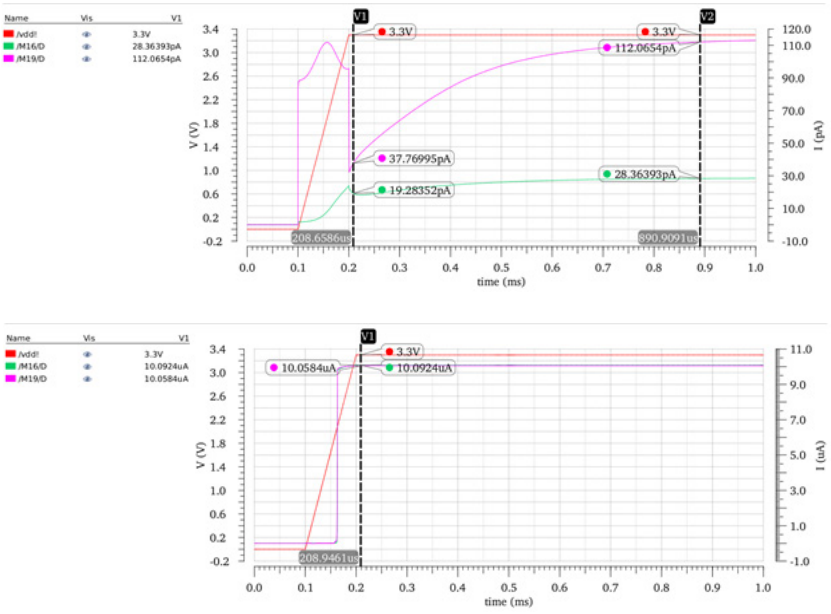

Fig. 3. Operation of the reference current source at power-up
without the start-up circuit (top) and with the start-up circuit (bottom)

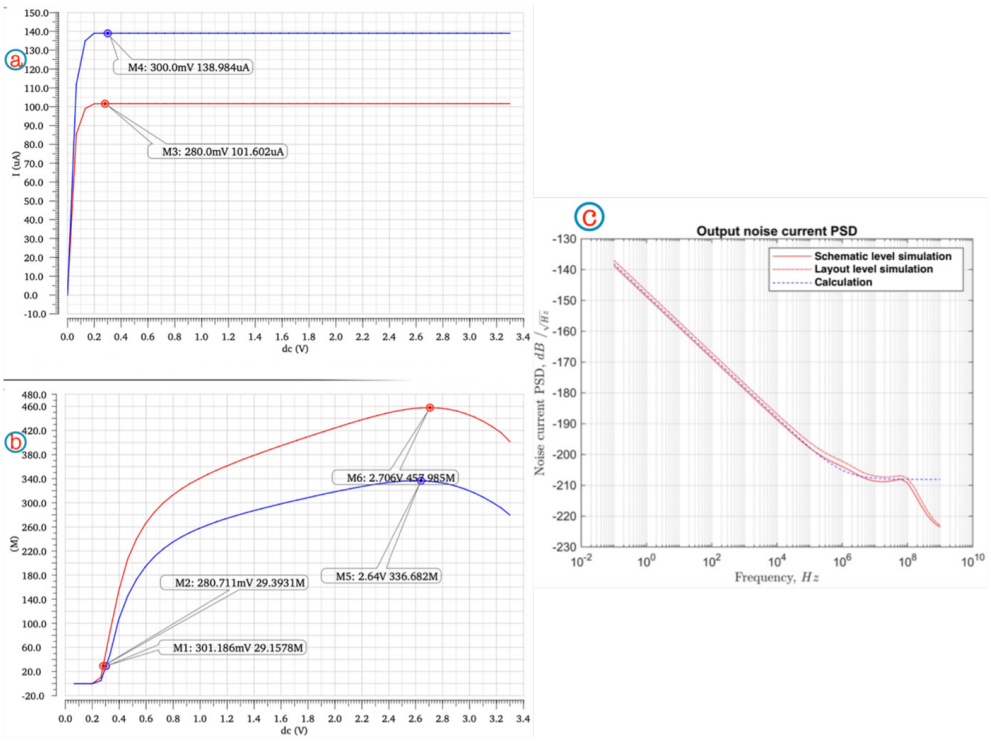

Fig. 4. Results of DC and noise analysis: I-V characteristics of the proposed current driver (*a*),
its output impedance (*b*), and deviation between calculated and simulated noise PSD (*c*).
Red curves represent circuit-level simulation, while blue curves correspond to layout-level simulation

characteristics in panel (Fig. 4, *a*) and comparing the calculated and simulated output noise current spectral densities in panel (Fig. 4, *b*). Note, there is close agreement between the schematic-level simulations (red curve) and the post-layout results (blue curve), with discrepancies not exceeding 2 dB

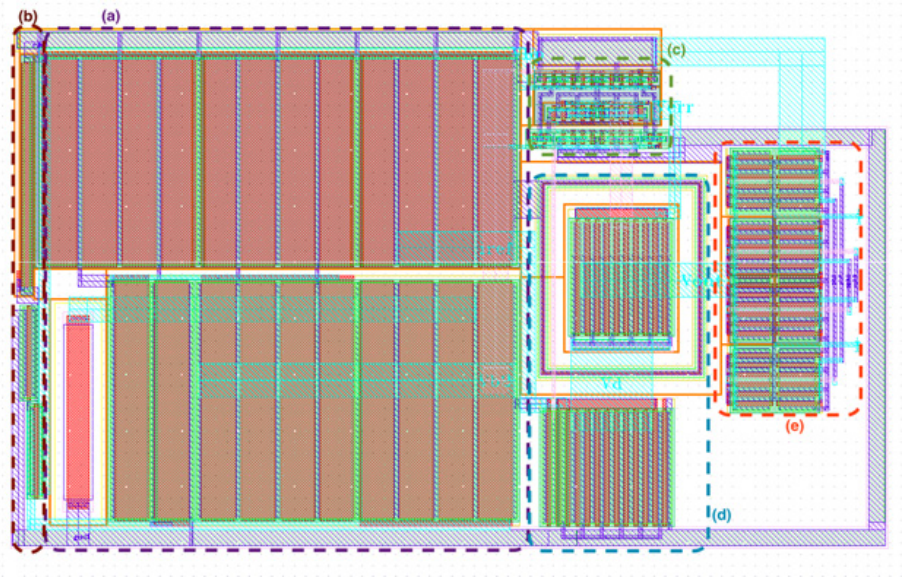

Fig. 5. Device layout: reference current source (*a*), start-up circuit (*b*), differential amplifier (*c*), current mirror ($K = 10$) (*d*), H-bridge (*e*)

within the frequency band of interest. This close correlation confirms that designers can reliably optimise the reference current source using these calculation methods, eliminating the need to simulate the complete circuit each time and significantly speeding up the design process.

The physical implementation is shown in Fig. 5 and demonstrates the robust performance of the circuit through several key specifications. The design generates a 140 μA output current from a 10 μA reference current while maintaining 90.9% voltage swing capability ranging from 300 mV to the full 3.3 V supply rail. The Op-Amp provides 54 dB of gain with a 190 kHz bandwidth, striking a balance between precision and speed. However, it should be noted that the output impedance exceeds requirements across much of the operational output voltage range. This performance margin stems from the inherent properties of the MOS transistors, as output impedance shows a strong dependence on overdrive voltage.

A more detailed examination of the circuit's behaviour reveals temperature stability, with output current variation of less than 0.1% per degree Celsius across typical temperature ranges (−40°C to 80°C). The amplifier maintains its 54 dB gain within 3 dB even at temperature extremes, demonstrating robust thermal performance.

Fig. 5 shows that transistors M42 and M44 are atypically arranged for cascading. This is due to the substrate current induced the body bias effect (SCBE) in the technology employed. To prevent the current from flowing into the substrate of transistor M42, its source and bulk terminals are shorted, and the transistor itself is isolated from the rest of the chip by a pn junction. This is the reason for the difference in the output current amplitude between schematic and layout level simulation.

It can be seen from the simulation results that the actual RMS noise at the output is more significant than ten times the noise of the reference current source assumed in the calculation of the rational output impedance, since only the contribution of the reference source has been taken into account. This provides a margin of output impedance in terms of feasibility with respect to noise level.

Comparison with the state of the art

Table 1 provides a detailed comparison of the key performance parameters of various implementations. References [1] and [4] have the highest output impedance, exceeding 1 GΩ, but require a large silicon footprint of over 0.2 mm^2. The ±9 V bipolar architecture in reference [5] enables superior

current programmability and load handling capability, making it particularly versatile for stimulation applications. However, this comes at a cost: operational power dissipation reaches 70 mW, and the implementation occupies a similar area to that of reference [4]. Furthermore, the design is unable to sustain consistent output impedance across its full current range, which limits its precision in certain operating regimes.

Table 1

Comparison with the state of the art

	[1]	[2], [6]	[4]	[5]	This paper
CMOS process	180 nm	IBM 130 nm	IBM 130 nm	180 nm	180 nm
Supply	bipolar, 5 V	3.3 V	bipolar, 3.3 V	bipolar, 9 V	3.3 V
Output impedance (R_{out})	1 GΩ	100 kΩ	320 GΩ	–	30 MΩ
Voltage range at the output (as a percentage of the supply voltage)	90%	60%	90.9%	91.1% Vdd	90.9% Vdd
Current amplitude	from 0.02 mA to 5.1 mA	from 0.01 mA to 1 mA	0.096 mA	from 0.032 mA to 10 mA	0.14 mA
IC area	0.5 mm^2	0.015 mm^2	0.2 mm^2	0.19 mm^2	>0.035 mm^2
Power consumption stand-by / stimulation	–	– / 1 mW	– / 0.6 mW	1 μW / 70 mW	0.1 mW / 0.4 mW

Reference [2] is the area-optimized extreme at just 0.015 mm^2, though this minimization compromises other critical specifications, including output impedance and voltage compliance. The proposed design strikes a balance between competing parameters. It reduces power consumption by 24% compared to [4], while delivering a higher output current. With a die area of less than 0.035 mm^2, it occupies 3 times more space than reference [2], but remains 5 times more compact than other implementations. The solution maintains more than 90% voltage utilization, which is comparable to that of [4], while providing 30 MΩ output impedance, which is sufficient for target applications. Further increases would not improve current stability, but would negatively impact area, power and complexity. This analysis shows that the implemented architecture successfully balances the fundamental design trade-offs between performance, size and efficiency in current source implementations.

Conclusion

The developed noise analysis methodology enables the calculation of the required current driver parameters and establishes a practical upper limit of 30 MΩ for output impedance under typical operating conditions. This threshold was determined using a reference current source that generated 3.4 nA RMS noise at a nominal current of 10 μA. The analysis shows that increasing the impedance value towards 100 GΩ provides diminishing returns in terms of current stability, while substantially increasing silicon area and power requirements.

The implemented circuit demonstrates measurable improvements over existing solutions in three critical areas: power efficiency, die area utilization and operational voltage range. Experimental results confirm stable operation with 30 MΩ output impedance, maintaining over 90% supply voltage utilization (300 mV to 3.3 V) when delivering a 140 μA output current. These specifications translate to a maximum supported load resistance of approximately 21 kΩ at full output current. The complete implementation occupies less than 3500 μm^2 of silicon area.

This balanced approach prioritizes practical performance metrics over theoretical maximums, recognizing that the excessive pursuit of ultra-high output impedance provides negligible benefits for actual current stability, while incurring significant implementation complexity costs. Instead, the design methodology focuses on achieving sufficient noise-limited performance within constrained area and power budgets, making it particularly suitable for applications where these practical considerations outweigh purely theoretical performance benchmarks.

The voltage-dependent output impedance characteristics suggest opportunities for adaptive biasing approaches in future iterations, particularly for applications requiring wide output ranges. While originally designed for precision current delivery, the architecture shows potential for scaling to higher current applications or adaptation to specialized fields like biomedical instrumentation, where its combination of precision and stability would be particularly valuable.

REFERENCES

1. **Rozgić D., Hokhikyan V., Jiang W., Akita I., Basir-Kazeruni S., Chandrakumar H.** A 0.338 cm^3, artifact-free, 64-contact neuromodulation platform for simultaneous stimulation and sensing. *IEEE Transactions on Biomedical Circuits and Systems*, 2019, Vol. 13, No. 1, Pp. 38–55. DOI: 10.1109/TBCAS.2018.2889040

2. **Abdelhalim K., Jafari H.M., Kokarovtseva L., Perez Velazquez J.L., Genov R.** 64-channel UWB wireless neural vector analyzer SOC With a closed-loop phase synchrony-triggered neurostimulator. *IEEE Journal of Solid-State Circuits*, 2013, Vol. 48, No. 10, Pp. 2494–2510. DOI: 10.1109/JSSC.2013.2272952

3. **Lee J., Rhew H.-G., Kipke D.R., Flynn M.P.** A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic ADC. *IEEE Journal of Solid-State Circuits*, 2010, Vol. 45, No. 9, Pp. 1935–1945. DOI: 10.1109/JSSC.2010.2052403

4. **Maghami M.H., Sodagar A.M., Sawan M.** Analysis and design of a high-compliance ultra-high output impedance current mirror employing positive shunt feedback. *International Journal of Circuit Theory and Applications*, 2015, Vol. 43, No. 12, Pp. 1935–1952. DOI: 10.1002/cta.2049

5. **Haas M., Vogelmann P., Ortmanns M.** A neuromodulator frontend with reconfigurable Class-B current and voltage controlled stimulator. *IEEE Solid-State Circuits Letters*, 2018, Vol. 1, No. 3, Pp. 54–57. DOI: 10.1109/LSSC.2018.2827885

6. **Kassiri H., Bagheri A., Soltani N., Abdelhalim K., Jafari H.M., Salam M.T.** Battery-less tri-band-radio neuro-monitor and responsive neurostimulator for diagnostics and treatment of neurological disorders. *IEEE Journal of Solid-State Circuits*, 2016, Vol. 51, No. 5, Pp. 1274–1289. DOI: 10.1109/JSSC.2016.2528999

7. **Wang Y., Luo H., Chen Y., Jiao Z., Sun Q., Dong L.** A closed-loop neuromodulation chipset with 2-level classification achieving 1.5-Vpp CM interference tolerance, 35-dB stimulation artifact rejection in 0.5ms and 97.8%-sensitivity seizure detection. *IEEE Transactions on Biomedical Circuits and Systems*, 2021, Vol. 15, No. 4, Pp. 802–819. DOI: 10.1109/TBCAS.2021.3102261

8. **Wang A., Jung D., Park J., Junek G., Wang H.** Electrode–electrolyte interface impedance characterization of ultra-miniaturized microelectrode arrays over materials and geometries for sub-cellular and cellular sensing and stimulation. *IEEE Transactions on NanoBioscience*, 2019, Vol. 18, No. 2, Pp. 248–252. DOI: 10.1109/TNB.2019.2905509

9. **Lempka S.F., Miocinovic S., Johnson M.D., Vitek J.L., McIntyre C.C.** In vivo impedance spectroscopy of deep brain stimulation electrodes. *Journal of Neural Engineering*, 2009, Vol. 6, No. 4, Art. no. 046001. DOI: 10.1088/1741-2560/6/4/046001

10. **Maghami M.H., Sodagar A.M., Sawan M.** Versatile stimulation back-end with programmable exponential current pulse shapes for a retinal visual prosthesis. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 2016, Vol. 24, No. 11, Pp. 1243–1253. DOI: 10.1109/TNSRE.2016.2542112

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