Computing, Telecommunication and Control, 2025, Vol. 18, No. 2, Pp. 91–98.
Информатика, телекоммуникации и управление. 2025. Том 18, № 2. С. 91–98.

Circuits and Systems for Receiving, Transmitting and Signal Processing

Устройства и системы передачи, приема и обработки сигналов

Short message
DOI: https://doi.org/10.18721/JCSTCS.18207
UDC 621.3.049.774.2

INCREMENTAL DELTA-SIGMA MODULATOR

M.M. Pilipko ✉ , *D.V. Morozov*

Peter the Great St. Petersburg Polytechnic University,
St. Petersburg, Russian Federation

✉ m_m_pilipko@rambler.ru

Abstract. A delta-sigma modulator with reset for incremental ΔΣ ADCs for the 180 nm CMOS technology with a supply voltage of 3.3 V from Mikron JSC is presented. The simulation of the ΔΣ modulator in the time domain in the Virtuoso analog design environment from Cadence DS was performed. The clock frequency was set to 6.25 MHz. The power consumption was about 9.5 mW. The reset was performed every 32 or 128 clock cycles. The results of the ΔΣ modulator simulation were processed in MATLAB. The digital decimation filter in the form of a cascade of integrators was realized in software. At the oversampling ratio of 32, the modulator shows SINAD = 69.3 dB (ENOB = 11.2 bits) and SFDR = 76.9 dB. At the oversampling ratio of 128, SINAD = 88.7 dB (ENOB = 14.4 bits) and SFDR = 92.7 dB are achieved. The crystal dimensions were 640 x 340 μm. The ΔΣ modulator circuit is suitable for precise digitization of sensor signals in the audio frequency range.

Keywords: analog-to-digital converter, delta-sigma modulator, incremental delta-sigma ADC, bootstrapped switch, dynamic element matching

Acknowledgements: The production of the integrated microcircuit was funded by the Ministry of Science and Higher Education of the Russian Federation within the framework of the federal project “Training of personnel and scientific foundation for the electronic industry” under the state assignment for the implementation of the research work “Development of a methodology for prototyping an electronic component base in domestic microelectronic production based on the MPW service”.

Citation: Pilipko M.M., Morozov D.V. Incremental delta-sigma modulator. Computing, Telecommunications and Control, 2025, Vol. 18, No. 2, Pp. 91–98. DOI: 10.18721/JCSTCS.18207

Краткое сообщение
DOI: https://doi.org/10.18721/JCSTCS.18207
УДК 621.3.049.774.2

ИНКРЕМЕНТАЛЬНЫЙ ДЕЛЬТА-СИГМА МОДУЛЯТОР

М.М. Пилипко ✉ , *Д.В. Морозов*

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

✉ m_m_pilipko@rambler.ru

Аннотация. Представлен ΔΣ модулятор со сбросом для инкрементальных ΔΣ АЦП по 180 нм КМОП-технологии с напряжением питания 3,3 В от АО «Микрон». Моделирование ΔΣ модулятора во временной области проводилось в среде аналогового проектирования Virtuoso компании Cadence DS. Тактовая частота была равна 6,25 МГц. Потребляемая мощность составила около 9,5 мВт. Сброс производился каждые 32 или 128 тактов. Результаты моделирования ΔΣ-модулятора обрабатывались в MATLAB. Цифровой децимирующий фильтр в виде каскада интеграторов реализован программно. При коэффициенте передискретизации 32 модулятор обеспечивает SINAD = 69,3 дБ (ENOB = 11,2 бит) и SFDR = 76,9 дБ. При коэффициенте передискретизации 128 достигаются SINAD = = 88,7 дБ (ENOB = 14,4 бит) и SFDR = 92,7 дБ. Размеры кристалла составили 640x340 мкм. Схема ΔΣ модулятора пригодна для точной оцифровки сигналов датчиков физических величин в звуковом диапазоне частот.

Ключевые слова: аналого-цифровой преобразователь, дельта-сигма модулятор, инкрементальный дельта-сигма АЦП, ключ с постоянным сопротивлением, динамическое согласование элементов

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию на выполнение научно-исследовательской работы «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW».

Для цитирования: Pilipko M.M., Morozov D.V. Incremental delta-sigma modulator // Computing, Telecommunications and Control. 2025. Т. 18, № 2. С. 91–98. DOI: 10.18721/JCSTCS.18207

Introduction

For battery-powered systems, such as sensors, power-efficient analog-to-digital converters (ADCs) are especially important and are typically tuned to the required bandwidth. Incremental delta-sigma (ΔΣ) ADCs [1, 2] are the optimal choice for achieving high power efficiency. Incremental ΔΣ ADCs have a reset and perform a sample-by-sample conversion, which distinguishes them from traditional ΔΣ ADCs, when digitizing weakly correlated input samples. Since such converters typically have a finite impulse response, the corresponding decimation filter can be as simple as a cascade of integrators, which is much simpler than their counterparts using filters with an infinite impulse response.

The block diagram of such an ADC is shown in Fig. 1. It consists of a ΔΣ modulator, a decimation filter and a reset circuit. The input signal X is fed to the ΔΣ modulator. At the ΔΣ modulator output, an oversampled digital data stream Y is formed, which is processed by the decimation filter. At the output of the digital decimation filter, the ΔΣ ADC output code D is formed. The clock signal (clk) is fed both to the ΔΣ modulator and the reset circuit. The reset circuit is a counter that is controlled by an oversampling ratio signal (OSR) – 32 or 128 in this paper – and discretely changes the conversion

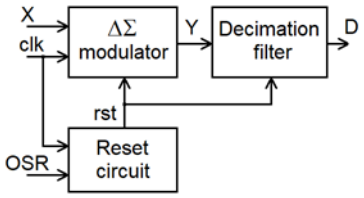

Fig. 1. Incremental ΔΣ ADC

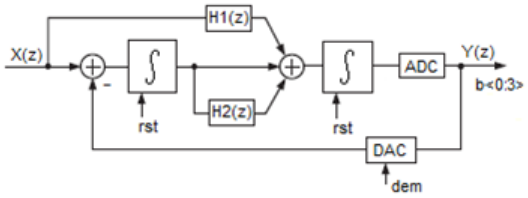

Fig. 2. The second-order ΔΣ modulator with reset

factor within the oversampling ratio values and generates a reset signal (rst). This paper will focus on the design of the ΔΣ modulator with the reset for incremental ΔΣ ADCs.

Functional-level model of the ΔΣ modulator

Fig. 2 shows a functional-level model in z-domain [3, 4] of the second-order ΔΣ modulator with reset, which consists of two integrators with reset, feedforward paths $H1(z) = H2(z) = 1-z^{-1}$, two analog adders, a quantizing circuit in the form of an ADC, and a digital-to-analog converter (DAC) in the negative feedback loop. Unlike other modulator structures, this structure requires only one feedback DAC and does not require an adder before the local ADC. The input is designated as X(z). The digital data stream b<0:3> is formed at the output Y(z) of the ΔΣ modulator. The first integrator has a transfer function $z^{-1}/(1-z^{-1})$, and the second integrator has a transfer function $0.5/(1-z^{-1})$. Both integrators are reset by the "rst" signal every 32 or 128 clock cycles. The feedback DAC suffers from mismatch of component values. In order to alleviate this problem, a dynamic elements matching (DEM) circuit in DAC is developed [5]. The signal for controlling the DEM part of the DAC is designated as "dem".

Cadence Virtuoso circuit of the ΔΣ modulator

According to the functional level block diagram of the ΔΣ modulator shown in Fig. 2, *a* circuit of the ΔΣ modulator based on switched capacitors has been developed in the Virtuoso analog design environment from Cadence DS. The circuit of the ΔΣ modulator with reset is shown in Fig. 3, where the 180 nm complementary metal-oxide-semiconductor (CMOS) technology with a supply voltage of 3.3 V from Mikron JSC was used. The ΔΣ modulator layout is shown in Fig. 4. Sizes of the layout are 640×340 um.

In Fig. 3, input signals – non-inverting (inp) and inverting (inm) – are applied to the integrators via bootstrapped switches [6, 7]. Each integrator utilizes a folded-cascode rail-to-rail operational transconductance amplifier (OTA) similar to [5, 8], with the width of the transistors in OTA1 being two times greater than the width of the transistors in OTA2 due to a proportionally larger load. The OTA inputs are non-inverting (vp) and inverting (vm), the OTA outputs are non-inverting (vop) and inverting (vom). The signal equal to half the supply voltage is designated as "vcm". The output signals of the integrators are "o1m" and "o1p" for the first integrator and "o2m" and "o2p" for the second integrator.

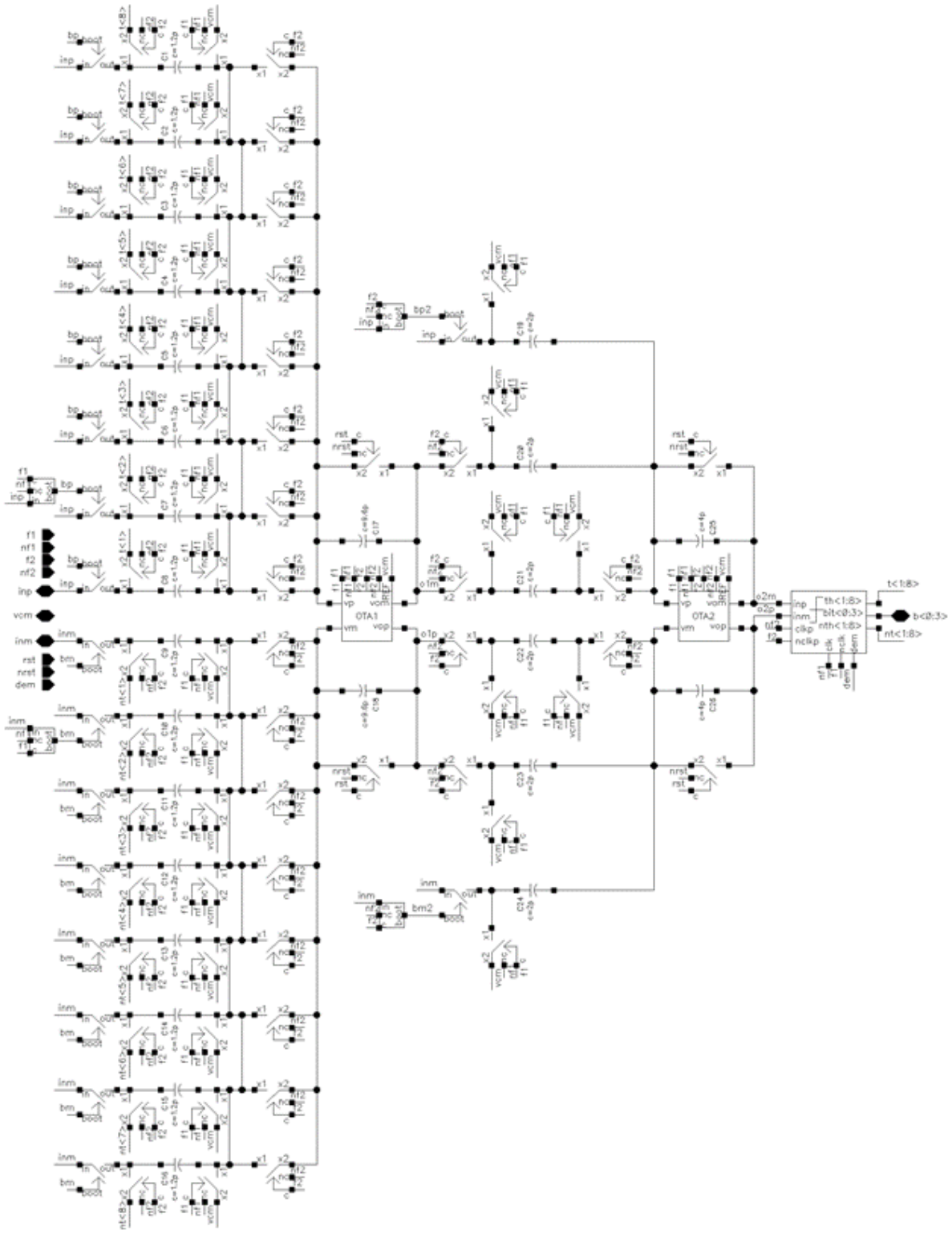

Fig. 3. The ΔΣ modulator in Virtuoso by Cadence DS

The quantizer at the output of the ΔΣ modulator forms four output bits b<0:3> and has eight quantization levels, which are provided by comparators similar to [5]. The non-inverting and inverting feedback signals of the ΔΣ modulator are presented in thermometer code and are designated by t<1:8> and nt<1:8>, respectively. The signal for controlling the dynamic elements matching circuit [5] is designated

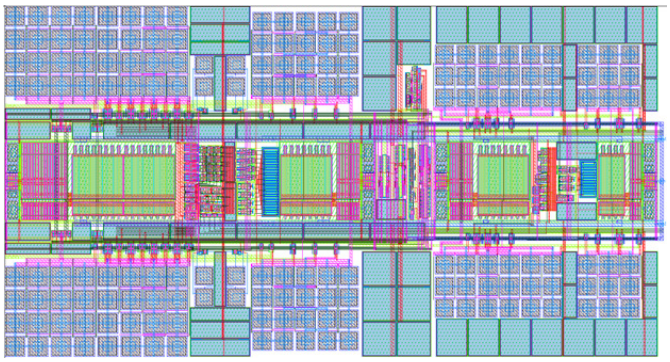

Fig. 4. The ΔΣ modulator layout

as “dem”. The circuit uses CMOS switches controlled by two phase sequences “f1” and “f2” similar to [5]. Phase sequences “nf1” and “nf2” are inverted to “f1” and “f2”, respectively. The main feature of this ΔΣ modulator circuit is the presence of CMOS switches that perform reset of the integrators by connecting the input and the output of the OTA pairwise using the “rst” signal (“nrst” is the inverse signal to “rst”).

The input capacitance of the ΔΣ modulator consists of eight parallel-connected capacitors with a nominal value of 1.2 pF to both non-inverting (inp) and the inverting (inm) inputs, which totally gives 9.6 pF in both of the specified nodes. Capacitors with a nominal value of 9.6 pF are connected in the feedback loops of OTA1. This ratio of capacitances sets the unity gain in the first integrator of the ΔΣ modulator. The load of the first integrator is the input capacitance of the second integrator, which in total is 4 pF at both the non-inverting (vop) and inverting (vom) outputs of OTA1. Capacitors with a nominal value of 4 pF are connected in the feedback loops of OTA2. Each of the capacitors connected to both the non-inverting (vp) and the inverting (vm) inputs of OTA2 has a nominal value of 2 pF. This ratio of capacitances sets the gain of 1/2 in the second integrator of the ΔΣ modulator. With these ratios of capacitances, the circuit of the ΔΣ modulator corresponds to its z-domain transfer function in the functional-level model described in previous section.

The ΔΣ modulator circuit in Virtuoso by Cadence DS was simulated at 27°C in the time domain with transient noise option turned on. The clock frequency was set to 6.25 MHz. The input harmonic signal frequency was 1335 Hz, the amplitude was 1 V. Power consumption was 9.5 mW. The simulation results were processed in MATLAB. The input differential signal “inp” and “inm”, reset signal (rst) and output code b<0:3> in decimal form (DSM code) are shown in Fig. 5 for the case when the “rst” signal acts every 32 clock cycles. The ΔΣ modulator output code in decimal form takes values from 0 to 8. After the reset pulse on the second graph, the code at the output of the ΔΣ modulator takes the value 4, which corresponds to the middle of the specified range of the output values.

Processing the simulation results of the ΔΣ modulator in MATLAB

The results of the time-domain simulation of the ΔΣ modulator were processed in MATLAB. A software implementation was done for the decimation filter from Fig. 1 in the form of a cascade of integrators. The number of the integrators in the decimating filter is two, which corresponds to the order of the ΔΣ modulator.

For the case when the reset signal (rst) acts every 32 clock cycles, the output code after processing by the digital decimation filter is shown in Fig. 6, *a*. Every 32 clock cycles, the sum of the ΔΣ modulator output codes is formed by accumulation. The resulting digital values before the reset moment proportionally represent the shape of the input harmonic analog signal. Fig. 6, *b* shows the decimated output code of the digital filter fixed in the register before the reset moment. In decimal form, the

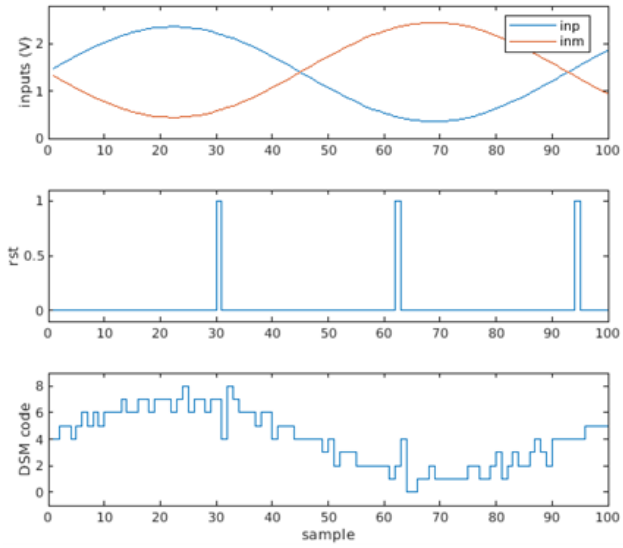

Fig. 5. Simulation results of the ΔΣ modulator from Virtuoso by Cadence DS processed in MATLAB

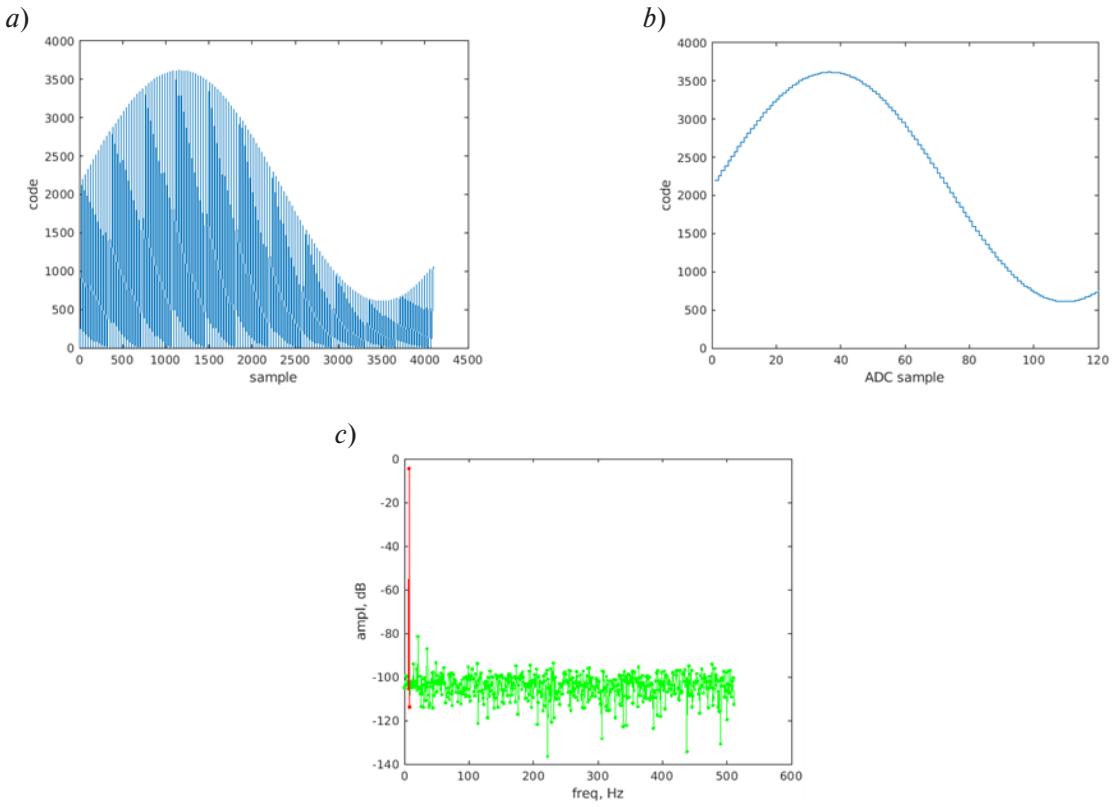

Fig. 6. Processing in MATLAB the simulation results for the reset signal (rst) acting every 32 clock cycles

values of the decimation filter output code range from 608 to 3616. The decimation filter output code spectrum is shown in Fig. 6, *c*, a 1024-point discrete Fourier transform with a rectangular window was performed. The calculated signal-to-noise and distortion ratio is SINAD = 69.3 dB (the effective number of bits is ENOB = 11.2 bits), spurious-free dynamic range is SFDR = 76.9 dB.

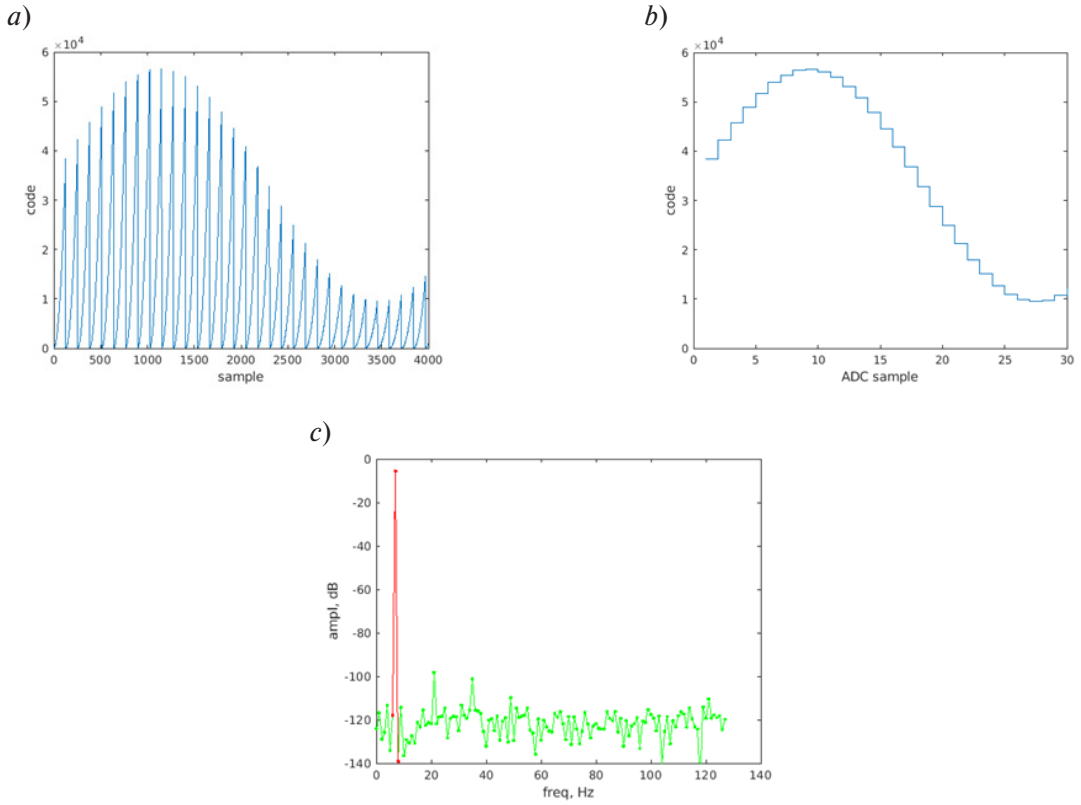

Fig. 7. Processing in MATLAB the simulation results for the reset signal (rst) acting every 128 clock cycles

For the case when the reset signal (rst) acts every 128 clock cycles, the output code after processing by the decimation filter in the form of the cascade of integrators is shown in Fig. 7, *a*. Every 128 clock cycles, the sum of the ΔΣ modulator output codes is formed by accumulation. The clock frequency and the input harmonic signal are the same as in the previous case.

Fig. 7, *b* shows the output code of the decimation filter fixed in the register before the reset moment. In decimal form, the values of the decimation filter output code range from 9466 to 56584. The decimation filter output code spectrum is shown in Fig. 7, *c*, a 256-point discrete Fourier transform with a rectangular window was performed. The calculated characteristics are SINAD = 88.7 dB (ENOB = 14.4 bits) and SFDR = 92.7 dB.

Conclusions

Delta-sigma modulators are suitable for relatively low-frequency applications, such as sensor systems and audio applications, that require high-quality digitization of the input signal. Unlike traditional ΔΣ ADCs, incremental ΔΣ ADCs allow easy integration into multi-channel systems due to sample-by-sample digitization without memory effect.

The ΔΣ modulator with reset for incremental ΔΣ ADCs was designed in 180 nm CMOS technology with a supply voltage of 3.3 V from Mikron JSC. The clock frequency is set to 6.25 MHz. Power consumption is about 9.5 mW. The reset acted every 32 or 128 clock cycles, i.e., the signal band was from 0 to either 195 kHz or 49 kHz, respectively. When the reset acts every 32 clock cycles, circuit properties are as follows: SINAD = 69.3 dB (ENOB = 11.2 bits), SFDR = 76.9 dB. With the reset at every 128 clock cycles, SINAD = 88.7 dB (ENOB = 14.4 bits) and SFDR = 92.7 dB. This allows the ΔΣ modulator to be used in precision measurement systems.

REFERENCES

1. **Tan Z., Chen C.-H., Chae Y., Temes G.C.** Incremental delta-sigma ADCs: A tutorial review. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2020, Vol. 67, No. 12, Pp. 4161–4173. DOI: 10.1109/TCSI.2020.3033458

2. **Satyshev V.I.** Modern approaches to design of multi-channel delta-sigma ADCs. *Computing, Telecommunications and Control*, 2022, Vol. 15, No. 2, Pp. 25–31. DOI: 10.18721/JCSTCS.15202

3. **San H., Konagaya H., Xu F., Motozawa A., Kobayashi H., Ando K.** Second-order ΔΣAD modulator with novel feedforward architecture. *50th Midwest Symposium on Circuits and Systems*, 2007, Pp. 148–151. DOI: 10.1109/MWSCAS.2007.4488558

4. **Honarparvar M., de la Rosa J.M., Sawan M.** A 0.9-V 100-μ W feedforward adder-less inverter-based MASH ΔΣ modulator with 91-dB dynamic range and 20-kHz bandwidth. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2018, Vol. 65, No. 11, Pp. 3675–3687. DOI: 10.1109/TCSI.2018.2854220

5. **Pilipko M.M., Morozov D.V., Yenuchenko M.S.** MASH 2-2 delta-sigma modulator with dynamic element matching in 0.18 μm CMOS technology. *Computing, Telecommunications and Control*, 2023, Vol. 16, No. 3, Pp. 29–38. DOI: 10.18721/JCSTCS.16303

6. **Razavi B.** The bootstrapped switch [A circuit for all seasons]. *IEEE Solid-State Circuits Magazine*, 2015, Vol. 7, No. 3, Pp. 12–15. DOI: 10.1109/MSSC.2015.2449714

7. **Kim S.-H., Lee Y.-H., Chung H.-J., Jang Y.-C.** A bootstrapped analog switch with constant on-resistance. *IEICE Transactions on Electronics*, 2011, Vol. E94.C, No. 6, Pp. 1069–1071. DOI: 10.1587/transele.E94.C.1069

8. **Pilipko M.M., Morozov D.V., Yenuchenko M.S.** Delta-sigma modulator with 10 MHz clock frequency in 180 nm CMOS technology. *MES-2018*, 2018, Pp. 44–48. DOI: 10.31114/2078-7707-2018-4-44-48

INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Pilipko Mikhail M.
Пилипко Михаил Михайлович
E-mail: m_m_pilipko@rambler.ru
ORCID: https://orcid.org/0000-0003-3813-6846

Morozov Dmitry V.
Морозов Дмитрий Валерьевич
E-mail: dvmorozov@inbox.ru
ORCID: https://orcid.org/0000-0003-3403-0120

Submitted: 17.03.2025; Approved: 24.05.2025; Accepted: 30.05.2025.
Поступила: 17.03.2025; Одобрена: 24.05.2025; Принята: 30.05.2025.