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A PIPELINE ANALOG-TO-DIGITAL CONVERTER IN 180 NM CMOS

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Abstract. A pipelined analog-to-digital converter (ADC) is presented, which was designed using 180 nm complementary metal-oxide semiconductor (CMOS) technology with a supply voltage of 1.8 V from Micron JSC. The ADC circuit consists of a sample-and-hold device, an 8-level redundant stage, five 6-level redundant pipeline stages, a back-end 3-bit ADC, as well as synchronization circuits, an adder and multiplexers to get at the output the 16-bit direct binary code of the whole ADC or the redundant code from first to fifth stages. The pipeline is implemented as a switched-capacitor circuit using operational transconductance amplifiers. The simulation of the ADC in the time domain in the Virtuoso analog design environment from Cadence DS was performed. The clock frequency was set to 50 MHz. The power consumption was about 52 mW, the following main characteristics were achieved: SINAD = 74.6 dB (ENOB = 12 bits) and SFDR = 75.3 dB.

Keywords: analog-to-digital converter, pipeline ADC, bootstrapped switch, time interleaving, redundant stage

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КОНВЕЙЕРНЫЙ АНАЛОГО-ЦИФРОВОЙ ПРЕОБРАЗОВАТЕЛЬ ПО ТЕХНОЛОГИИ КМОП 180 НМ

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Аннотация. Представлен конвейерный аналого-цифровой преобразователь (АЦП), который выполнен по 180 нм комплементарной металл-оксид-полупроводник (КМОП) технологии с напряжением питания 1,8 В от компании АО «Микрон». Схема АЦП состоит из устройства выборки и хранения, каскадов с избыточностью (8 уровней квантования в первом каскаде, 6 уровней в каскадах 2–6), оконечного АЦП с разрядностью 3 бита, а также схем синхронизации, сумматора и мультиплексоров для вывода либо прямого 16-разрядного двоичного кода, либо кода каскадов с избытком. Конвейер реализован как схема на переключаемых конденсаторах с использованием операционных транскондуктивных усилителей. Моделирование АЦП во временной области проводилось в среде аналогового проектирования Virtuoso компании Cadence DS. Тактовая частота была равна 50 МГц. Потребляемая мощность составила около 52 мВт, были достигнуты следующие основные характеристики: SINAD = 74,6 дБ (ENOB = 12 бит) и SFDR = 75,3 дБ.

Ключевые слова: аналого-цифровой преобразователь, конвейерный АЦП, ключ с постоянным сопротивлением, временное перемежение, каскад с избыточностью

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию на выполнение научно-исследовательской работы «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW».

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Introduction

For the implementation of precision high-speed analog-to-digital converters (ADCs), the most promising one is the currently widely used pipeline architecture. On one hand, pipelined ADCs provide a higher resolution with a lower power consumption compared to flash ADCs. On the other hand, pipelined ADCs operate at higher frequencies compared to successive-approximation ADCs [1]. Therefore, these ADCs offer a compromise between the achieved resolution and the operating frequency. The pipelined ADCs are used in applications, such as high-definition video, wireless local area networks etc. [2, 3].

A typical pipelined ADC consists of a sample-and-hold (S/H) device and a number of ADC stages connected in series one after another. The first stage of the pipelined ADC allows to determine the most significant bits of the ADC output code. The next stages of the pipeline sequentially determine the next significant bits of the ADC output code. A stage contains a low-resolution ADC (usually a flash ADC of 1–4 bits) and a multiplying digital-to-analog converter (DAC). One of the possible approaches to realize the DAC is the use of a switched-capacitor circuit.

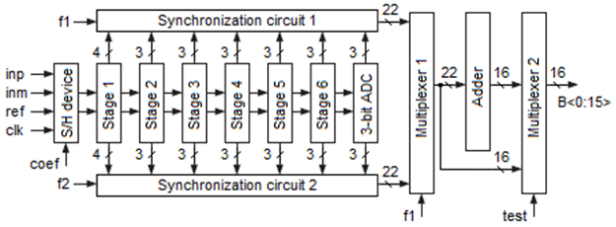


Fig. 1. Block diagram of the pipelined ADC

The paper presents a block diagram of the designed pipelined ADC and discusses the implementation of its blocks based on a complementary metal-oxide-semiconductor (CMOS) technology. A specialized computer-aided design system was used to obtain simulation results and define the main characteristics of the pipelined ADC.

Block diagram of the pipeline ADC

Fig. 1 shows a block diagram of the pipelined ADC. The differential input signal ("inp" and "inm") is fed to the S/H device, whose gain is discretely set as 1 or 2 by the signal "coef". The clock frequency of the S/H device is set by the clock signal (clk). The signal "ref" corresponds to the voltage of the direct current (DC) operating point for the input signals ("inp" and "inm"). The S/H device can process both a differential input signal and the non-differential signal at the input "inp", in the latter case the signal "ref" should be fed to the input "inm".

The differential signal from the output of the S/H device is fed to sequentially connected pipeline stages. In the pipeline, interleaving is organized within two half-periods of the clock signal, which are designated as phases "f1" and "f2". The first stage of the pipeline has a 4-bit output from the flash ADC with 8 comparators. Each of the following five stages has a 3-bit output from its flash ADC with 6 comparators. The output of the sixth stage is fed to the back-end flash ADC with 7 comparators and 3 output bits. Compared to a basic 2-bit stage, the implemented pipeline stages provide redundancy in the representation of the output code. The output signals of the stages and the 3-bit ADC are delayed by the required number of clock signal periods using synchronization circuits 1 and 2. As a result, codes that correspond to a respective input sample are properly arranged.

The signals from the outputs of the synchronization circuits are fed to the multiplexer 1, which is controlled by phase "f1" at the address input. When the phase signal "f1" takes the value 1, the output signal of the synchronization circuit 1 appears at the output of the multiplexer 1. During the time when the phase signal "f1" takes the value 0 (phase "f2" is actually in effect), the output signal of the synchronization circuit 2 appears at the output of the multiplexer 1. This way the interleaving is realized in the digital part of the circuit.

The signal from the output of multiplexer 1 is fed to the adder, which performs summation taking into account the weight of the redundant codes at its inputs and generates the ADC output code. The multiplexer 2 at the ADC output, which is controlled by the test signal (test) at the address input, allows either the straight binary code from the adder output or 16 digits of the redundant code from first to fifth stages to pass to the circuit output. The latter option allows for off-chip correction of the interstage gain error and other ADC imperfections.

Cadence Virtuoso circuit of the pipelined ADC

The pipelined ADC based on switched capacitors has been developed in the computer-aided design system Virtuoso by Cadence DS, where the 180 nm CMOS technology with a supply voltage of 1.8 V from Mikron JSC was used. The layout of the pipelined ADC is shown in Fig. 2. Sizes of the layout are 1600×300 um.

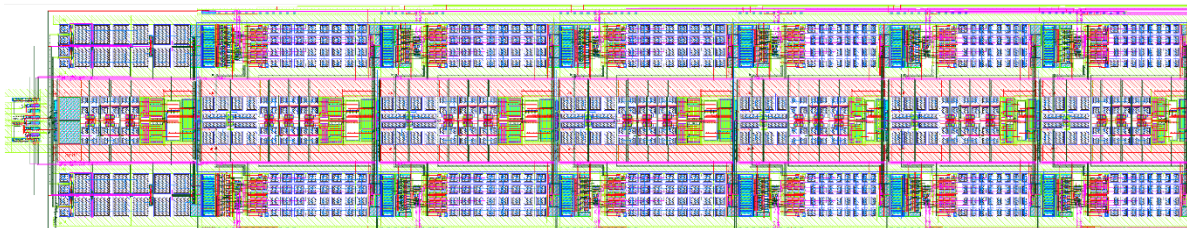


Fig. 2. Layout of the pipelined ADC

The circuit of the S/H device is shown in Fig. 3. Input signals (non-inverting “inp” and inverting “inm”) are applied to the circuit via bootstrapped switches [4, 5]. The S/H device is based on a folded-cascode rail-to-rail operational transconductance amplifier (OTA) similar to [6, 7], but with additional boosting amplifiers to increase the gain according to recommendations [8, 9]. According to the simulation results at 27°C, at a 7 pF load the DC gain of OTA1 is 91.5 dB, the unity-gain bandwidth is 335 MHz, the phase margin is 57 degrees, power consumption is 9.2 mW. The OTA inputs are non-inverting (vp) and inverting (vm), the OTA outputs are non-inverting (vop) and inverting (vom). The supply voltage is designated as “vdd!”. The circuit uses CMOS switches controlled by two non-overlapping phases “f1” and “f2” similar to [6]. Phases “nf1” and “nf2” are inverted to “f1” and “f2”, respectively. The S/H device outputs “outp” and “outm” are taken from the OTA outputs “vom” and “vop”, respectively.

Capacitors with a nominal value of 1.8 pF are connected in the feedback loops of OTA1. When the signal “coef” takes the value 0, the input capacitance of the S/H device consists of capacitors with a nominal value of 1.8 pF to both non-inverting (inp) and inverting (inm) inputs. This ratio of input and feedback capacitances sets the unity gain in the S/H device. When the signal “coef” takes the value 1, the input capacitance of the S/H device consists of two parallel-connected capacitors with a nominal value of 1.8 pF to both non-inverting (inp) and inverting (inm) inputs, which totally give 3.6 pF in each of the specified nodes. This sets a 2x gain in the S/H device. As seen, the OTA is used by the circuit only in phase “f1”. In phase “f2”, the OTA is used by an identical S/H device that samples the input in phase “f1”. This principle of operation allows for interleaving and effectively doubles the conversion rate of the ADC.

As said before, the S/H device [10] can convert a non-differential signal to a differential signal, which is preferable for the further analog-to-digital conversion. As can be seen from Fig. 3, there is a CMOS switch between the nodes “sw0p” and “sw0m” and a CMOS switch between the nodes “sw1p” and “sw1m”. Assume that a harmonic signal is fed to “inp”, while the signal “ref” (half the supply voltage “vdd!”) is fed to “inm”. The signal “coef” is set to 1. In the sample phase, the capacitors C1 and C2 have the same charge Qinp, which is different from the charge of capacitors C3 and C4. The latter ones have the voltage “ref” at both plates, thus, each of the capacitors C3 and C4 has the same charge equal to 0. In the hold phase, CMOS switches between nodes “sw0p” and “sw0m”, “sw1p” and “sw1m” are closed, and the Qinp charge of C1 is divided equally between capacitors C1 and C4, while the Qinp charge of C2 is divided equally between capacitors C2 and C3. Therefore, all capacitors have the same charge equal to Qinp/2. This coefficient of 1/2 is compensated by the 2x gain of the S/H device.

The S/H device was simulated at 27°C in the time domain. Simulation results for the case, when the S/H device converts a non-differential signal to a differential signal, are shown in Fig. 4. The clock frequency is set to 50 MHz. The input harmonic signal frequency at the input (inp) is set to 781.25 kHz, the amplitude is 600 mV. The signal “ref” is 900 mV DC. The S/H device output signals “vom” and “vop” are depicted in the second plot.

The circuit of the first stage in the pipeline is shown in Fig. 5. The resistive divider R0-R14 between the power supply node “vdd!” and the ground node “gnd!” sets 8 reference voltages from 375 mV to

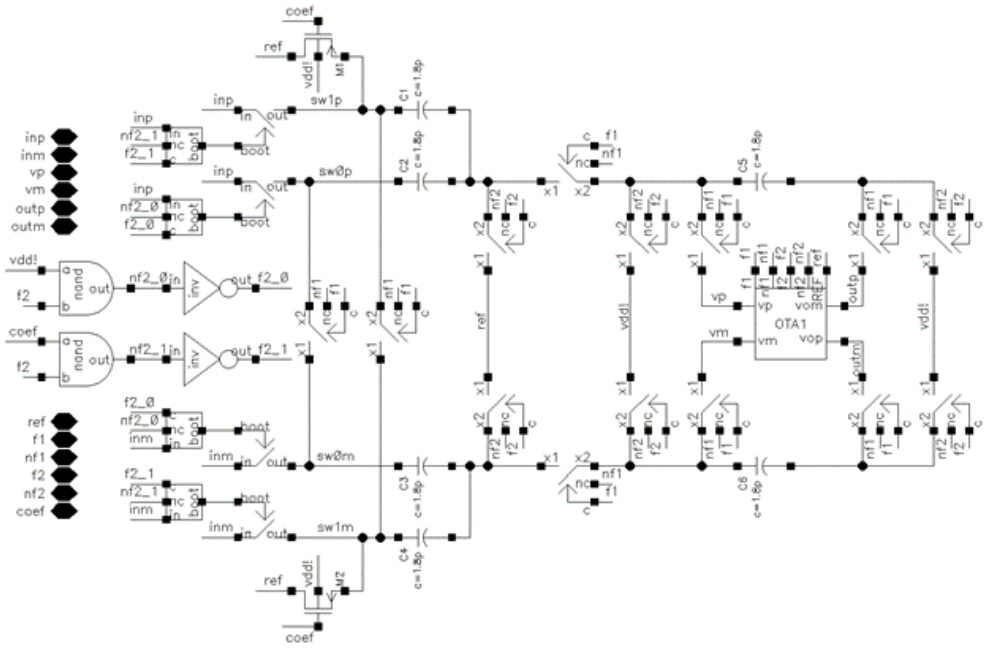


Fig. 3. S/H device in Cadence Virtuoso

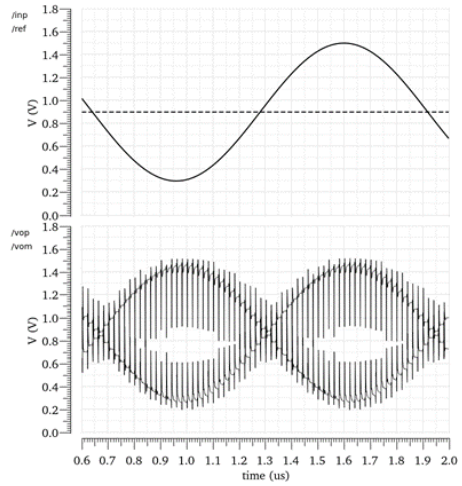
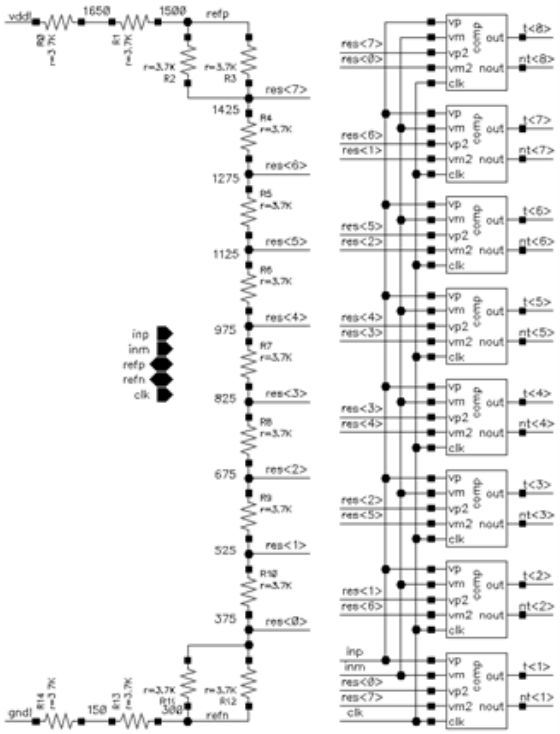


Fig. 4. Simulation results of the S/H device for the non-differential input signal

1425 mV in nodes “res<0:7>” for the comparators “comp” (Fig. 5, *a*). An excessive number of comparators allows for an extended voltage swing of the input signal that is limited by voltage levels 150 mV and 1.65 V. Differential comparator circuits similar to [6] are used. Input signals “inp” and “inm” are applied to the comparator inputs “vp” and “vm”, respectively. The reference voltages are fed to comparator inputs “vp2” and “vm2”. At the comparator outputs “out” and “nout”, direct and inverted codes of the comparison result are formed. The output thermometer code of the comparators is designated “t<0:7>” (the inverted code is “nt<0:7>”). The thermometer code is converted into a 4-bit direct binary output code of the first stage by an adder.

The input signals “inp” and “inm” are also applied to the switched-capacitor part of the first stage via bootstrapped switches (Fig. 5, *b*). The circuit also uses CMOS switches controlled by two phases

a)



b)

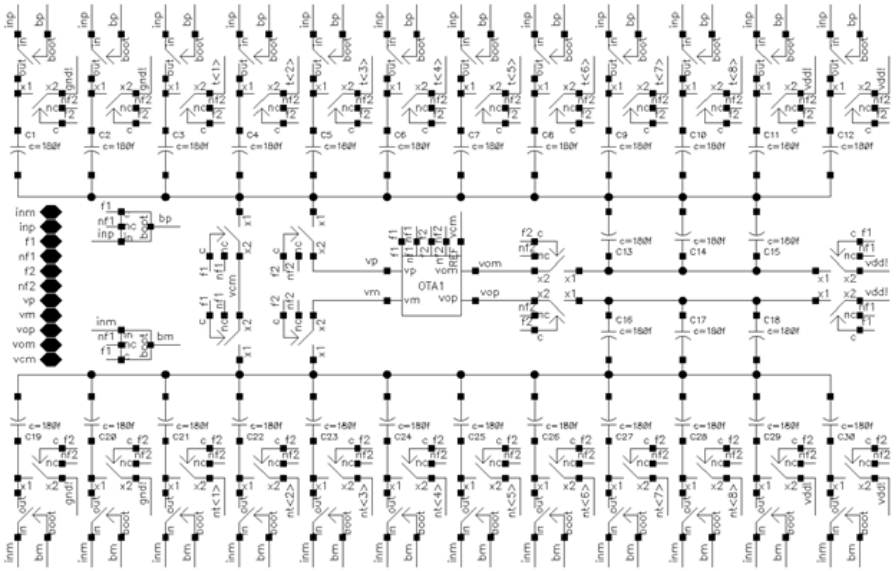


Fig. 5. First stage in Cadence Virtuoso

"f1" and "f2" (inverted "nf1" and "nf2" respectively). The first stage outputs are designated as "vop" and "vom". The input capacitance of the first stage consists of 12 parallel-connected capacitors with a nominal value of 180 fF to both "inp" and "inm", which totally give 2.16 pF in each of the specified nodes. In the feedback loops of OTA1 there are three capacitors with a nominal value of 180 fF connected in parallel, which totally give 540 fF. This ratio of capacitances sets a 4x gain in the first stage. Again, here the OTA is used by the circuit only in phase "f2". In phase "f1", this OTA is used by the interleaved ADC stage that samples the input in phase "f2".

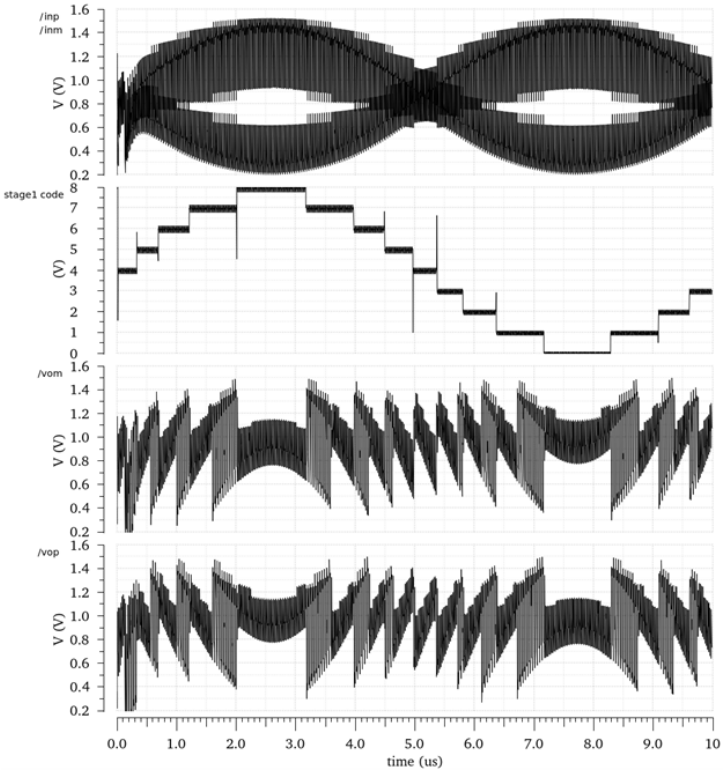


Fig. 6. Simulation results of the first stage

The output thermometer code of the comparators “t<0:7>” and “nt<0:7>” is fed to 8 of 12 CMOS switches in the corresponding branch of the switched capacitor circuit. The rest 4 of 12 switches are connected as follows: 2 switches – to the ground node “gnd!”, 2 switches – to the power supply node “vdd!”, which defines the voltage range of the DAC in the first stage between 300 mV and 1.5 V.

The first stage simulation results at 27°C in the time domain are depicted in Fig. 6. The differential input signal “inp” and “inm” of the first stage of the pipeline ADC is shown in the first plot. The second plot shows the 4-bit direct binary output of the first stage in decimal equivalent. At the output of the stage, a difference is formed between the differential input signal of the stage and the decimal equivalent of the output code. Two last plots show the output signals “vom” and “vop”, which are the input signals for the second stage of the pipelined ADC.

The remaining stages 2–6 of the pipelined ADC are similar to the first stage, the only differences are as follows. Each of the stages 2–6 has 6 comparators to form the 3-bit output code. The resistive divider R0-R14 (Fig. 5, *a*) sets 6 reference voltages from 525 mV to 1275 mV at nodes “res<1:6>” for the comparators. The output thermometer code of the comparators “t<1:6>” and “nt<1:6>” is fed to 6 of 12 CMOS switches in the corresponding branch of the switched-capacitor circuit (Fig. 5, *b*). The rest 6 of 12 switches are connected as follows: 3 switches – to the ground node “gnd!”, 3 switches – to the power supply node “vdd!”, which defines the operating voltage range of the DAC between 450 mV and 1350 mV. The stages 2–4 are based on OTA1, while stages 5 and 6 utilize OTA2, with the width of the transistors being two times less than the width of the transistors in OTA1. The back-end 3-bit ADC has a resistive divider that sets 7 reference voltages from 450 mV to 1350 mV, while 7 comparators form the 3-bit output code.

Power consumption of the pipelined ADC is near 52 mW. The output code spectrum of the pipelined ADC is shown in Fig. 7, a 512-point discrete Fourier transform with a rectangular window was performed. The calculated signal-to-noise and distortion ratio (SINAD) is 74.6 dB, i.e. the effective

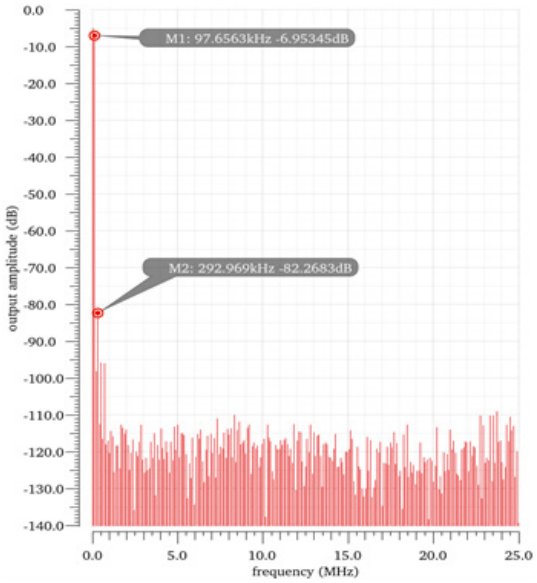


Fig. 7. Simulation results of the output code spectrum for the pipeline ADC

number of bits (ENOB) is 12 bits, spurious-free dynamic range (SFDR) is 75.3 dB. At a clock frequency of 5 MHz, SINAD is 78.8 dB, SFDR is 80.1 dB.

Conclusions

The pipelined ADCs are in demand in high-resolution high-speed applications. A 16-bit pipelined ADC was presented for 180 nm CMOS technology with a supply voltage of 1.8 V from Mikron JSC. Time interleaving was applied to effectively utilize the analog components and double the conversion rate. Pipeline stages use redundancy to compensate for the offset of comparators. Raw code of the pipeline stages is available at the outputs in the "test" mode, which makes further correction possible. The simulation of the ADC in time domain in the Virtuoso analog design environment from Cadence DS was performed. The clock frequency was set to 50 MHz. Power consumption was near 52 mW. For an input amplitude of 600 mV, SINAD = 74.6 dB (ENOB = 12 bits) and SFDR = 75.3 dB were achieved.

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