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DESIGN PROCESS OF THE MASH 2-2 SIGMA-DELTA MODULATOR

A.S. Kozlov[1] ✉, *M.M. Pilipko*[2], *A.T. Tulaev*[1], *Ya.V. Belyaev*[1]

[1] Concern CSRI Elektropribor, JSC, St. Petersburg, Russian Federation;

[2] Peter the Great St. Petersburg Polytechnic University, St. Petersburg, Russian Federation

✉ kas573@yandex.ru

Abstract. This paper presents the design process of the cascaded (MASH) 2-2 sigma-delta modulator. For this purpose, several sigma-delta modulator topologies were studied at the system and schematic levels. Simulation at the system level was used to define the requirements for the operational transconductance amplifier (OTA), which is a part of the integrator. Sigma-delta modulators were designed using a 0.18 μm CMOS technology library. The influence of temperature swing, process variations and noise on the characteristics of second-order sigma-delta modulators was taken into account during simulation. As a result of the simulation, the optimal second-order topology was selected. This topology was used to design the cascaded (MASH) 2-2 sigma-delta modulator. The developed modulator has a resolution of 15.97 effective bits, a working frequency band of 20 kHz, consumes 12 mW of power at a supply voltage of 3.3 V. The occupied area of the circuit on the chip is 0.22 mm^2. A device with such characteristics can be used in interfaces of micromechanical sensors.

Keywords: ADC, sigma-delta, OTA, comparator, topology

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РАЗРАБОТКА MASH 2-2 СИГМА-ДЕЛЬТА МОДУЛЯТОРА

А.С. Козлов[1] ✉ , *М.М. Пилипко*[2] ,
А.Т. Тулаев[1], *Я.В. Беляев*[1]

[1] АО «Концерн «ЦНИИ «Электроприбор», Санкт-Петербург, Российская Федерация;
[2] Санкт-Петербургский политехнический университет Петра Великого, Санкт-Петербург, Российская Федерация

✉ kas573@yandex.ru

Аннотация. В данной статье представлена разработка каскадного (MASH) 2-2 сигма-дельта модулятора. В ходе работы были рассмотрены различные архитектуры сигма-дельта модуляторов на системном и схемотехническом уровнях. Моделирование на системном уровне позволило определить характеристики операционного транскондуктивного усилителя (ОТУ), входящего в состав интегратора. Для разработки схемотехнической реализации сигма-дельта модуляторов использовалась технологическая библиотека КМОП-технологии с нормами 0,18 мкм. На схемотехническом уровне было проведено моделирование структур второго порядка с учетом шума, температуры, а также разброса параметров технологии. В результате моделирования была выбрана оптимальная структура второго порядка. На основе этой структуры была построена схема каскадного сигма-дельта модулятора. Разработанный модулятор имеет разрешающую способность 15,97 эффективных бит, полосу рабочих частот 20 кГц, занимает на кристалле площадь в 0,22 мм^2 и потребляет 12 мВт мощности при напряжении питания 3,3 В. Устройство с такими характеристиками может применяться в интерфейсах микромеханических датчиков и сенсоров.

Ключевые слова: АЦП, сигма-дельта, ОТУ, компаратор, топология

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Introduction

The rapidly growing market for microelectromechanical systems (MEMS) is driving the demand for precision interface chips. Analog-to-digital converters (ADCs) are an essential part of such circuits, since without them, further digital processing of the signal from the MEMS device is impossible. The output signals of MEMS sensors usually do not exceed tens of kilohertz, so ADCs based on sigma-delta (ΣΔ) modulation are most often used to convert them into digital form. A sigma-delta ADC consists of an analog (sigma-delta modulator) and a digital (filter-decimator) part. This type of ADC is capable of providing high resolution (up to 24 bits). Typically, sigma-delta ADCs consume much less power than faster ADC architectures. Sigma-delta ADCs achieve high resolution by using noise shaping and high sampling rates above the Nyquist frequency (oversampling).

Sigma-delta modulators can be roughly divided into two general categories: continuous-time (CT) and discrete-time (DT) circuits. In CT circuits, the only clocked unit is the comparator, while the integrator is implemented as a Gm-C, active RC or passive RC filter. Sigma-delta modulators of this type

consume less power and are capable of operating at higher clock rates than DT modulators. According to [1], the highest operating frequency band for the CT modulator achieved to date is 465 MHz, while for the DT modulator this value is only 40 MHz. However, CT modulators also have their drawbacks. First, they have increased sensitivity to jitter, since errors in the digital-to-analog converter (DAC) occur due to an unstable clock signal. In addition, delays in the DAC and quantizer can introduce additional poles in the signal transfer function (SiTF) and noise transfer function (NTF), which leads to degraded performance and possible instability of the modulator. This effect is called excess loop delay (ELD) [2].

In contrast, DT sigma-delta modulators have lower bandwidth and higher performance requirements for an operational amplifier, which is a part of an integrator. Nevertheless, they have become widespread due to their immunity to jitter and ELD. It is also worth noting that the characteristics of DT modulators are less sensitive to process variations.

Simulation of second-order topologies at system level

First-order sigma-delta modulators are easy to design and inherently immune to instability. Nevertheless, the relatively low level of the suppression of quantization noise at moderate values of the oversampling ratio significantly limits their scope of application. This is why second-order sigma-delta modulators have become the most widely used.

Interest in second-order sigma-delta modulators has led to the emergence of a number of different structures. The best known is Boser–Wooley modulator – cascade of integrators with feedback (CIFB) [3]. Reducing the gains of the integrators improves the stability of the modulator for signals with high amplitude, and the use of delaying integrators makes it possible to reduce the speed requirements for the operational transconductance amplifier (OTA). Integrators' gains are chosen such that $STF(z) = z^{-2}$ and $NTF(z) = (1 - z^{-1})^2$.

The so-called feedforward topology was first introduced in [4]. Some papers also referred to it as the ideal topology and the broadband topology. The main advantages are the reduced requirements for the signal swing of the OTA (since the integrator processes only the quantization noise), as well as an increased dynamic range. This modulator implements $STF(z) = 1$ and $NTF(z) = (1 - z^{-1})^2$.

Another version of the sigma-delta modulator, called the cascade of integrators with distributed feedback topology with capacitive input feedforward (CIFB-CIF), was presented in [5]. The proposed modifications made it possible to reduce the speed requirements for the modulator components (it is especially important in the case of a modulator with a multi-bit quantizer, since in this case a multi-bit DAC with digital element matching is used), and also to omit the adder before the quantizer. Like the feedforward topology, this modulator implements $STF(z) = 1$ and $NTF(z) = (1 - z^{-1})^2$.

The following structure was first considered in [6]. A similar structure was published in [7].

It can be noted that this architecture is also characterized by the absence of an adder in front of the comparator. In addition, the modulator has only one feedback branch, therefore, to implement this structure, a single DAC is required, which makes it possible to reduce the area of the circuit on the chip, as well as power consumption. In this structure, $STF(z) = 1$ and $NTF(z) = (1 - z^{-1})^2$.

It is also possible to design a topology with $STF(z) = z^{-1}$ and $NTF(z) = (1 - z^{-1})^2$. This topology was considered in [8]. A hybrid topology is a kind of CIFB architecture. The hybrid topology, like the feedforward one, is characterized by reduced requirements for integrator nonlinearities. In addition, in this case, the number of signal branches is smaller and there is no adder in front of the comparator, therefore the power consumed by the modulator is reduced.

The noise performance of second-order topologies can be a limiting factor for their use in high-precision applications. Higher order sigma-delta modulators present an effective way to reduce quantization noise in signal band. The main drawback of high-order single-loop architectures is their vulnerability to instability. Multi-stAge noise SHaping (MASH) architecture can be immune to instability, while

demonstrating noise suppression comparable to high-order single-loop sigma-delta modulator. This is why MASH topologies are of interest.

Theoretically, any of the second-order topologies mentioned above can be used to design a MASH 2-2 sigma-delta modulator. However, different non-idealities should be taken into account. This is why simulation at a system level is an essential part of the design process. In [9, 10], an analysis of the influence of various factors on the performance of the first-order sigma-delta modulator was carried out. Nevertheless, the authors note that such an analysis needs to be performed for various architectures. In this regard, the effect of the finite gain, the finite gain-bandwidth and the finite slew rate will be discussed.

According to [11, 12], the finite value of the gain leads to an effect called "integrator leakage". The parameter p, which characterizes this effect, is defined as:

$$p = \frac{k-1}{k},$$

where k is the amplifier gain. Due to leakage, the gain of the integrator turns out to be different from the nominal value. It should also be noted that leakage changes the position of zeros in the noise transfer function, thereby increasing the noise power in the useful frequency band. These effects can greatly affect the operation of sigma-delta modulators based on the MASH architecture.

The influence of the gain bandwidth on the transfer function of the integrator was considered in [13]. Taking into account the gain bandwidth modifies the transfer functions as follows:

Non-inverting integrator:

$$H(z) = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}\left[1 - e^{-k_1}\left(\frac{C_1}{C_1 + C_2}\right)\right].$$

Inverting integrator:

$$H(z) = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}}\left[1 - e^{-k_1} + e^{-k_1}\left(\frac{C_2}{C_1 + C_2}\right)\right],$$

$$k_1 = \pi\left(\frac{C_2}{C_1 + C_2}\right)\left(\frac{f_t}{f_s}\right),$$

where f_t is the unity gain frequency, f_s is the clock frequency, C_1 is the input capacitor, C_2 is the feedback capacitor.

In practice, in switched-capacitor circuits, it is recommended to use amplifiers with gain bandwidth of at least 5 times the clock signal frequency [14, 15].

The slew rate (SR) of the op-amp output is also an important parameter that determines the overall performance of the sigma-delta modulator. The finite SR causes the gain to be nonlinear [11]. To account for this parameter, changes in the output signal are described using the equations from [16].

To implement a high SR, it is necessary to increase the current of the amplifier output stage. This leads to an increase in power consumption and an increase in the occupied area on the chip (due to wider devices). It is also possible to increase the SR by using class AB output stage amplifiers; however, these are difficult to design and generally require frequency compensation.

According to [17], the SR requirements are highly dependent on the gain bandwidth. To achieve high signal-to-noise-and-distortion ratio (SNDR) values, it is necessary to provide one of two operating modes of the integrator: slow or fast.

The normalized SR is determined by the expression:

$$SR_N = SR\frac{T_s}{2V_{pp}},$$

where T_s is the clock period, V_{pp} is the value of the feedback signal of the sigma-delta modulator (determined by the supply voltage).

In the slow mode, it is assumed to use an amplifier with a relatively small gain bandwidth (few times of f_s). The normalized SR in this mode must exceed the value of n_τ, which is defined as follows:

$$n_\tau = \frac{T_s}{2\tau},$$

where τ is the amplifier's time constant

$$\tau = \frac{1}{2\pi f_t}.$$

When working in this mode, two difficulties arise. First, a high SR is required for a broadband amplifier to operate correctly. Satisfying this criterion is especially problematic if the amplifier is loaded with a large capacitance. Second, if the gain bandwidth of the amplifier is higher than expected after the circuit is fabricated, the SR_N may occur less than n_τ, which will lead to a decrease in the SNDR of the modulator.

To implement a circuit operating in a fast mode, an amplifier with a bandwidth such that $n_\tau > 12$ is required. In this case, the SR requirements are significantly reduced.

To summarize all of the above, it should be noted that for each sigma-delta modulator topology, system-level models with OTA's non-idealities were designed. The model for the feedback topology is shown in Fig. 1.

The simulation results show that for $f_t = 20f_s$ the dependence of the SNDR on the amplitude of the input signal becomes close to ideal (with an infinitely high gain) when the normalized SR is higher than 5.

Similar dependencies were obtained for a finite gain and finite gain-bandwidth. All considered sigma-delta modulator topologies have shown approximately the same results.

System-level simulations show that for the MASH 2-2 modulator with SNDR > 90dB, input signal bandwidth of 20 kHz and oversampling ratio of 128, non-idealities of an OTA become negligible (do not degrade overall modulator performance) if its parameters meet the following requirements:

- DC gain of more than 40 dB;
- Gain bandwidth of more than 100 MHz;
- Slew rate of more than 82.5 V/us.

Simulation of the second-order topologies at the schematic level

In order to design second-order sigma-delta modulators at the schematic level, several main blocks are required: a CMOS switch, a comparator, and an OTA. The switch has a finite resistance, which, in the case of using a single transistor with a certain type of conductivity, turns out to be highly dependent on the input signal level. Using a switch based on a complementary pair of transistors allows one to effectively cope with this problem. The clock feedthrough effect, however, remains. One of the options for reducing the clock feedthrough is to use a CMOS switch with additional dummy transistors [18].

A comparator is required to convert the signal from the integrator output to a pulse train. Clocked comparators are of interest because they do not consume static power. An example of such a comparator

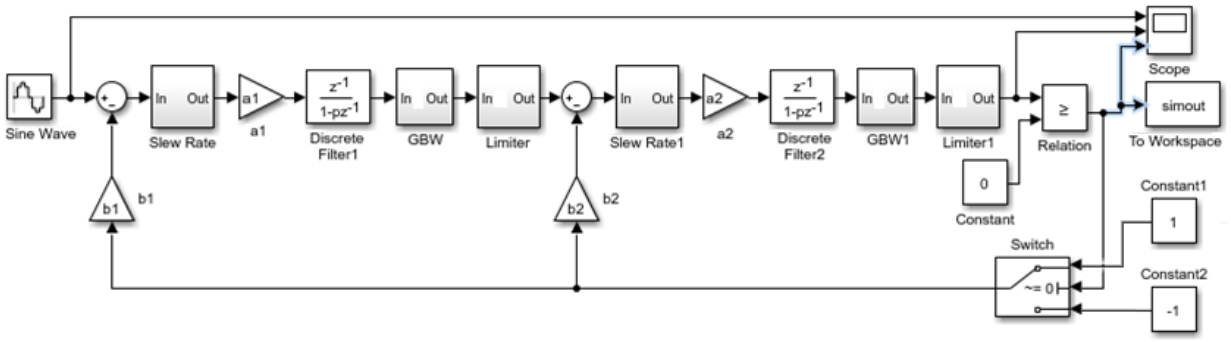

Fig. 1. System-level model of the feedback topology sigma-delta modulator

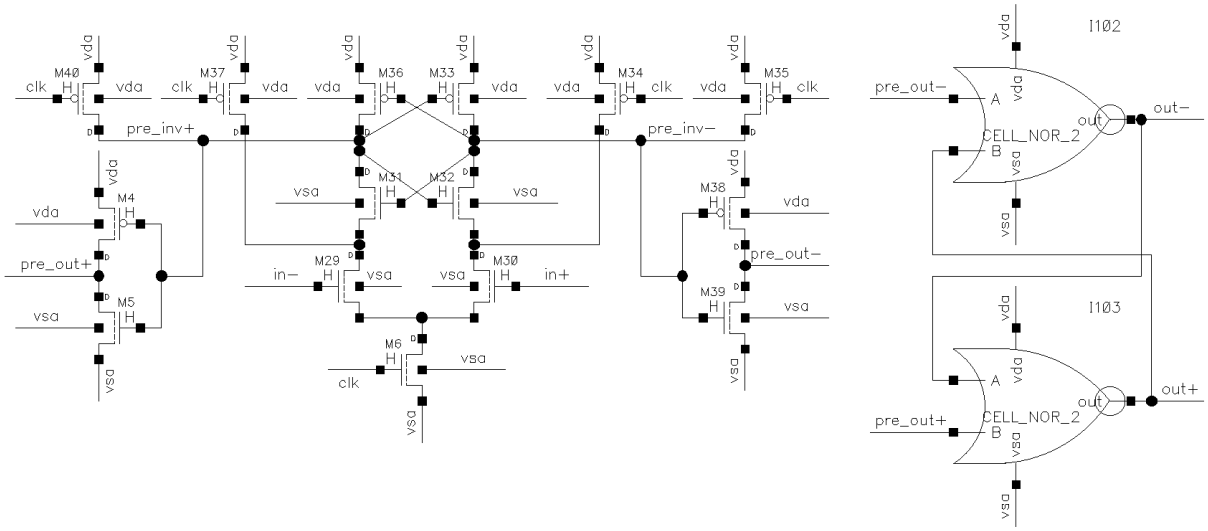

Fig. 2. StrongARM latch

is a structure called StrongARM latch [19], shown in Fig. 2. When a low-level signal is applied to the clock inputs of the comparator, the p-transistors connected in parallel with the bistable cell in the upper part of the circuit are turned on, and the current source in the form of an n-transistor in the lower part of the circuit is locked. As a result of resetting the comparator value, a logical zero value is set at both its outputs, regardless of the signals at the comparator inputs. In order to store the information signal while the comparator is reset, an RS-latch is used.

In the previous paragraph, the following OTA's requirements were obtained: DC gain of more than 40 dB, gain bandwidth of more than 100 MHz, slew rate of more than 82.5 V/us. In addition, in order to ensure high linearity, the OTA should have a rail-to-rail output signal swing. A folded-cascode amplifier meets these requirements. The amplifier with feedforward compensation from [20] was taken as a basis. For better stabilization of the operating point, a common mode feedback circuit (CMFB) in the form of a differential amplifier with diode-connected transistors as a load was used. Fig. 3 shows the final OTA schematic. Simulation results showed that the designed OTA has the following characteristics: DC gain of 75 dB, gain bandwidth of 200 MHz and slew rate of 102 V/us with a capacitive load of 4 pF. Performance margin is added in order to ensure the reliability of the design across all process corners.

After designing the main blocks, the design of the sigma-delta modulators themselves follows. Based on the analysis carried out earlier, an implementation with switched capacitors was chosen. All structures are fully differential.

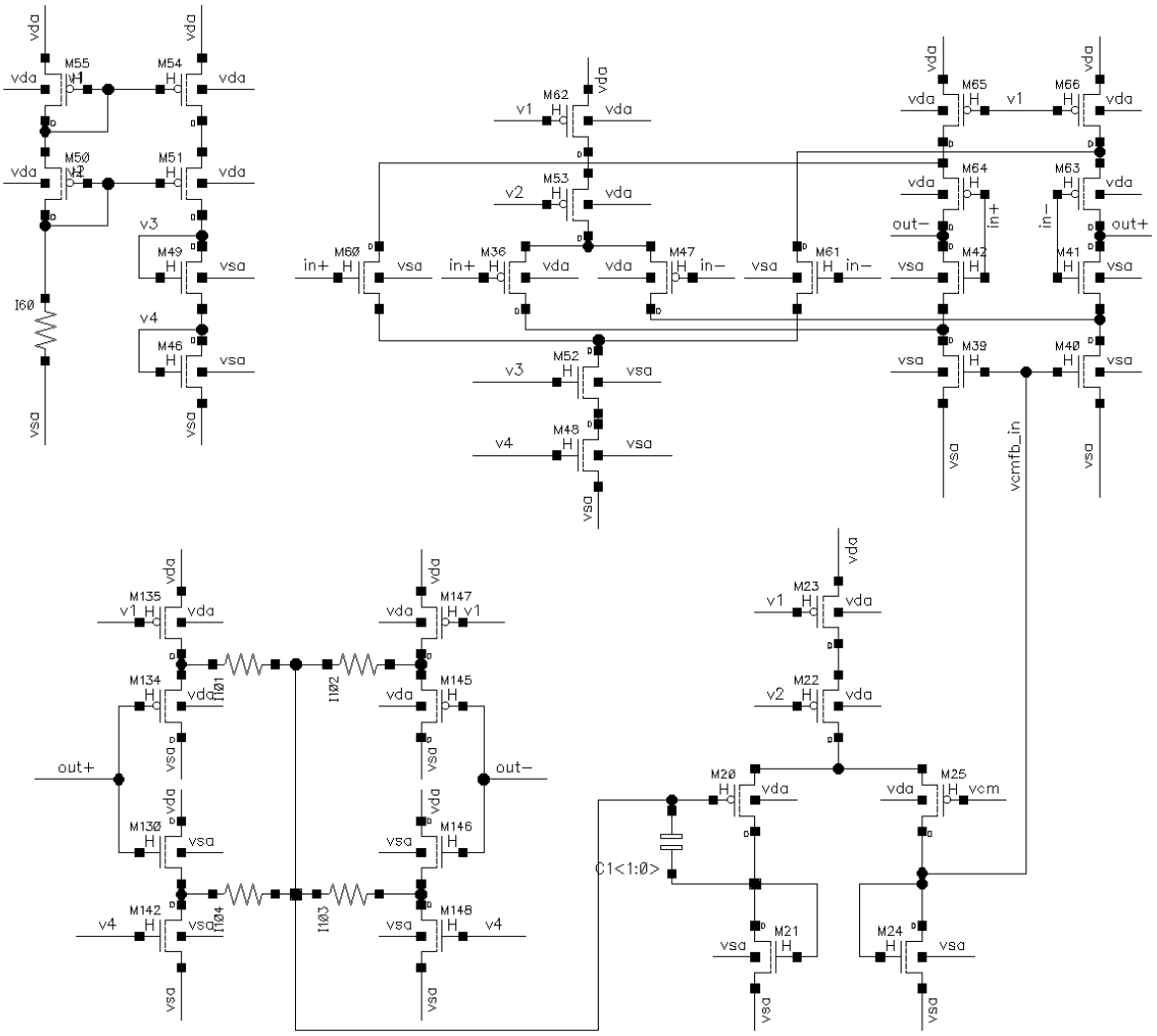

Fig. 3. Folded-cascode OTA

As a result of the simulation, the dependence of the SNDR of the output signal versus the amplitude of the input signal was obtained for different second-order topologies (Fig. 4). The graphs for feedback (FB), feedforward (FF [4]), hybrid (HY [21]), Gharbiya (GH [5]) and Murayama (MU [6]) topologies are shown.

Next, the simulation was carried out taking into account the influence of temperature swing, process variation and the intrinsic electrical noise of the circuit. Further simulation was carried out at a single signal amplitude of 1.2 V.

To study the effect of temperature on the characteristics of modulators, three temperature values were chosen: –40°C, 27°C, 85°C. Based on the data obtained, it can be concluded that the Murayama structure [6] is the most sensitive to the effect of temperature: the decrease in SNDR at the temperature of –40°C was 24 dB compared to the nominal value.

The technology libraries used in the project allow for simulation with process variations. The largest deviations of the parameters from the nominal values are called “corners”. The simulation showed that for all five structures, the change in characteristics turns out to be insignificant.

Simulation with intrinsic noise was performed using the transient noise option. The SNDR value for the Murayama structure decreased by 24 dB, for the Gharbiya structure – by 6.4 dB, and for the

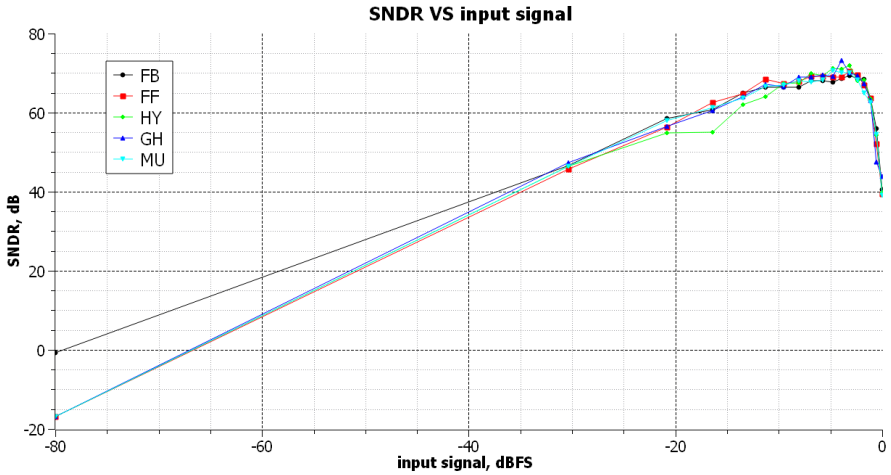

Fig. 4. SNDR vs input signal amplitude for different second-order topologies

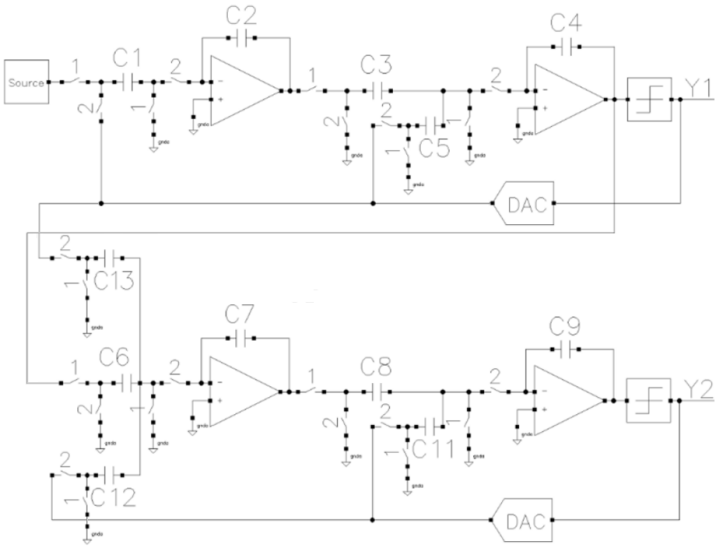

Fig. 5. Analog part of the MASH 2-2 sigma-delta modulator

feedforward structure – by 2.5 dB. The SNDR value for the feedback and hybrid structures even improved slightly after adding noise.

According to the simulation results, it is clear that the most reliable structures are the feedback, feedforward, and hybrid. In addition, as the feedback structure requires the least number of capacitors, it was decided to build the MASH sigma-delta modulator based on it.

The MASH 2-2 sigma-delta modulator

Next, the schematic of MASH 2-2 sigma-delta modulator was designed. The analog part is shown in Fig. 5. The first stage is presented by the feedback topology shown earlier. In the second stage, changes were made to this circuit. The modulator feedback is implemented using a separate capacitor C12. Capacitors C6 and C13 are used to subtract the code of the first stage from its residue analog signal. Signals Y1 and Y2 are then fed to the digital processing circuit. The resulting multibit signal has the properties of fourth-order noise shaping.

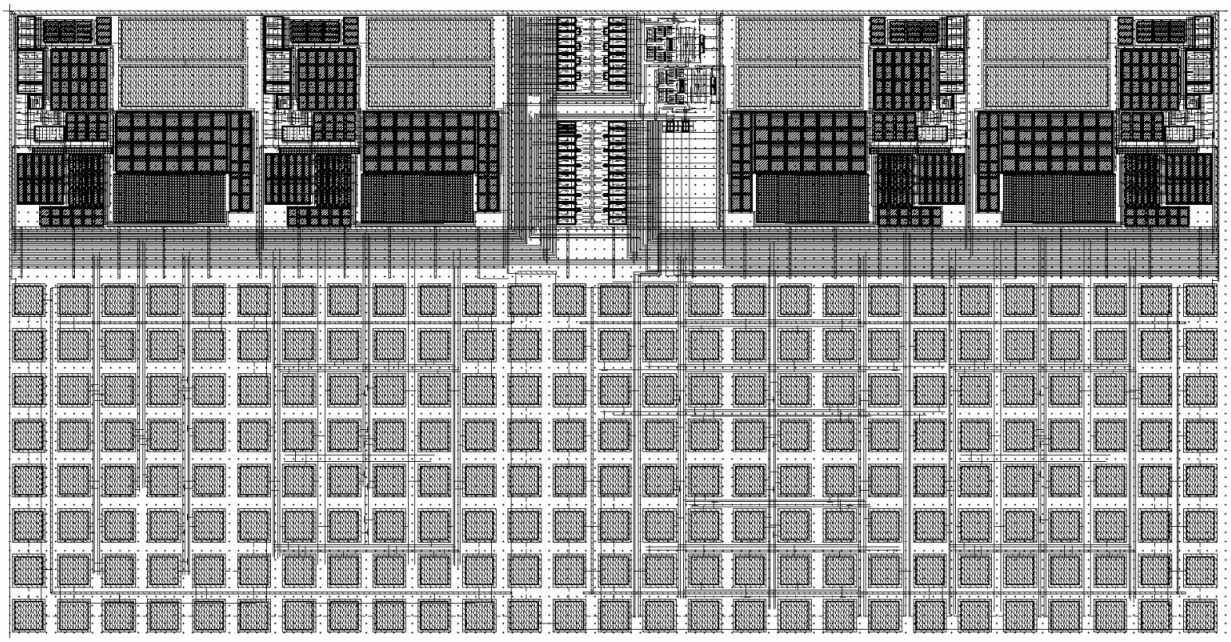

Fig. 6. The layout of the MASH 2-2 modulator core

The digital processing circuit is built based on adders and D-flip-flops. The output of the circuit is a parallel 5-bit digital code. The least significant bit is taken from the output of one of the D-flip-flops, the other bits are signals at the outputs of the adders. One of the inputs of the last adder is set to logic one in order to ensure that there are no negative values in the code.

The simulation of the MASH 2-2 sigma-delta modulator at the schematic level showed that the designed circuit can achieve an SNDR value of 97 dB.

The assembled layout of the MASH 2-2 sigma-delta modulator is presented in Fig. 6. The capacitor arrays and switches are seen in the bottom part while four OTAs, two comparators and the digital part are placed in the upper part. Overall characteristics of the designed modulator are as follows:

- Effective number of bits: 15.97;
- Power consumption: 12 mW (at a supply voltage of 3.3 V);
- Signal band: 20 kHz;
- Chip area: 0.22 mm^2.

Table 1 shows the comparison of the designed circuit with circuits from previous publications.

Table 1

Main parameters summary and comparisons

	This work	**[22]**	**[23]**	**[24]**	**[25]**
DR (bit)	15.97	17.9/14.8	12.29	14.49	14.32
BW, kHz	20	8000/20000	20000	20	20
OSR	128	20/8	12.5	128	100
Architecture	2-2	2-2-1	2-2	2-2	2-2
Supply voltage, V	3.3	3.3	1.2	0.9	1
Power, mW	12	68	20.4	0.065	0.66

Conclusion

The paper presents the design process of the MASH 2-2 sigma-delta modulator. Simulation at the system level was used to define the requirements for the requirements for the operational amplifier, which is the key building block of the sigma-delta modulators.

The circuits of the main blocks of a sigma-delta modulator based on a 0.18 μm CMOS technology library have been designed, and simulation has been carried out. Based on the developed blocks, five structures of second-order sigma-delta modulators were assembled, simulated and compared. The influence of temperature swing, process variations and noise on the characteristics of second-order sigma-delta modulators was taken into account during simulation. Simulation results showed that the feedback topology is the most suitable for implementing a cascaded sigma-delta modulator.

A schematic for the MASH 2-2 sigma-delta modulator has been designed, and the characteristics of the developed device have been obtained. With an effective number of bits equal to 15.97 in a signal band of 20 kHz, the circuit is suitable for audio systems and other high-resolution low-power applications.

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INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Kozlov Alexey S.
Козлов Алексей Сергеевич
E-mail: kas573@yandex.ru

Pilipko Mikhail M.
Пилипко Михаил Михайлович
E-mail: m_m_pilipko@rambler.ru
ORCID: https://orcid.org/0000-0003-3813-6846

Tulaev Artyom T.
Тулаев Артем Толибович
E-mail: artulaev@gmail.com

Belyaev Yakov V.
Беляев Яков Валерьевич
E-mail: jak0b@mail.ru

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