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INFLUENCE ANALYSIS OF COMPARATOR PARAMETERS SPREAD ON DECISION ACCURACY IN DAC SELF-CALIBRATION CIRCUIT

M.S. Yenuchenko ●, N.V. Kvashina ●, I.M. Piatak [≥]

Peter the Great St. Petersburg Polytechnic University, St. Petersburg, Russian Federation

 \mathbb{Z} i.m.piatak@gmail.com

Abstract. The article presents an analysis of the influence of the comparator parameter spread in the digital-to-analog converter (DAC) self-calibration circuit on the reduction of the conversion nonlinearity. DAC on sources with a switching-based self-calibration circuit is considered. The comparator response threshold value due to the spread of component parameters for 0.18 µm CMOS technology (HCMOS8D by "Mikron") is estimated. The comparator response threshold values are obtained for three sizes of comparator components. Functional modeling of the switching calibration taking into account the finite threshold of element comparison showed that the choice of the sorting algorithm affects the reduction of the conversion nonlinearity. It should be noted that for the smallest comparator option, only quick sort can provide an improvement in the integral nonlinearity for all considered conditions. The optimal size of the comparator components is determined in terms of the efficiency of nonlinearity reduction. The quick sort algorithm shows the best results both in nonlinearity reduction and in the influence of the comparator switching threshold sign.

Keywords: digital-to-analog converter, current source, switching-based calibration, mismatch, comparator threshold, elements sorting

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АНАЛИЗ ВЛИЯНИЯ РАЗБРОСА ПАРАМЕТРОВ КОМПАРАТОРА НА ТОЧНОСТЬ ПРИНЯТИЯ РЕШЕНИЯ В ЦЕПИ САМОКАЛИБРОВКИ ЦАП

М.С. Енученко ●, Н.В. Квашина ●, И.М. Пятак [⊠]

Санкт-Петербургский политехнический университет Петра Великого, Санкт-Петербург, Российская Федерация

✉ i.m.piatak@gmail.com

Аннотация. Представлен анализ влияния разброса параметров компаратора в цепи самокалибровки цифро-аналогового преобразователя (ЦАП) на снижение нелинейности преобразования. Рассмотрен цифро-аналоговый преобразователь на источниках с цепью коммутационной самокалибровки. Проведена оценка величины порога срабатывания компаратора, обусловленного разбросом параметров компонентов для технологии КМОП 0.18 µm («Микрон» HCMOS8D). Получены значения порогов срабатывания компаратора для трех размеров компонентов компаратора. Функциональное моделирование коммутационной калибровки с учетом конечного порога сравнения элементов показало, что выбор алгоритма сортировки влияет на снижение нелинейности преобразования. При этом отметим, что для наименьшего варианта компаратора только быстрая сортировка может обеспечить улучшение интегральной нелинейности для всех рассматриваемых условий. Определен оптимальный размер компонентов компаратора с точки зрения эффективности снижения нелинейности. Наилучшие результаты как по снижению нелинейности, так и по влиянию знака порога переключения компаратора показывает алгоритм быстрой сортировки.

Ключевые слова: цифро-аналоговый преобразователь, источник тока, коммутационная калибровка, рассогласование, порог компаратора, сортировка элементов

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Introduction

High-resolution digital-to-analog converters (DACs) impose strict requirements for components matching in order to provide sufficient linearity of conversion. For resolutions higher than 12 bits, the common approach to improve component matching is an electronic calibration. The calibration process includes analysis phase when component values or their ratios are assessed and the information about actual values of elements is used to minimize conversion nonlinearity. For this purpose, switching-based calibrations changes a manner of element switching [1–5].

As switching-based calibration aims to reduce part of analog blocks in favor of digital ones, a comparator is employed for analysis of element values [6–9]. The accuracy of matching assessment depends on the threshold of comparison determined by comparator properties. One of dominant factors that determine comparator threshold is a spread of its component parameters. However, there are no researches examining the effect of mismatch in the comparator on calibration results. This paper focuses

Fig. 1. Structure of a switching-based calibration circuit

Fig. 2. Time diagrams of a sorting phase

on assessing the influence of parameters on the accuracy of decision making in terms of the self-calibration circuit.

Calibration structure

This paper focuses on a switching-based self-calibration of current-steering DACs. One of the main phases in the switching-based calibration is a sorting phase. During this phase, an ascending (or descending) order of elements is established in accordance with their actual values. After that, a sorted order of elements is used to setup a new elements switching order for minimizing integral nonlinearity (INL). Fig. 1 shows the general structure of such a calibration circuit. The key component of such a calibration performing an assessment of element values is a comparator. A sorting procedure is the following. During the calibration stage, two elements under comparison are switched off from the DAC output and connected to the comparator's input. The comparator waits for the end of switching transition in one clock cycle and compares values of the current sources in the next clock cycle. Fig. 2 illustrates the described process. An obtained decision is used by sorting algorithm for swapping (or not) of elements. Wrong decision from the comparator may break partially or entirely the sorted order of elements.

Comparator circuit

In this paper, a dynamic comparator is considered [10]. It consists of resistor pair, differential amplifier and RS-trigger circuit. Schematics of comparator blocks are depicted in Fig. 3–5. The comparator is designed with 0.18 µm "Mikron" HCMOS8D technology. The current of two elements under comparison is converted into a voltage with resistor pair (I10, Fig. 5). Then their difference is amplified (Fig. 3) and is stored in the RS-trigger (I10, Fig. 4) as a digital signal ("0" or "1"). The comparator is designed to have a nominal current value at the center of supply voltage range. The considered current sources are based on a schematic of cascode current mirror with transistor sizes of 5 μ m/4 μ m and 16× multiplier.

Fig. 3. Amplifier block

Fig. 4. Amplifier with digital RS-trigger

Process variations effect the properties of transistor and make them different from the nominal values. As the result, the left and right branches become different, and comparator threshold drifts from zero. The effect induced by deviations can be reduced by an increase of components area. Therefore, the optimal area of comparator's components is a matter of concern. The present work investigates this issue in terms of subsequent effects of mismatch on the correctness of sorted order.

Simulation

The following approach is considered for a simulation of the comparator threshold. There are two current sources: one with the constant current value, another changes its current around the value of the first one. A difference between input voltages at the comparator's input, when the output changes, defines the comparator threshold. A Monte-Carlo simulation with 1000 runs is used to collect statistics of threshold value. Moreover, as components' area affects their matching properties and consequently threshold, different area of transistors in the comparator is considered (area of the resistors has not been changed). Simulation results are presented in Fig. 6 and in Table 1.

The threshold has approximately zero mean value as expected and covers both negative and positive values. The standard deviation of the threshold decreases with components' area increase. However, this

Fig. 5. Comparator block

dependency has the saturation and the threshold deviations do not noticeably (3%) decrease, when the transistor sizes increase by 5 times from 20 μ m/10 μ m to 100 μ m/50 μ m. Whereas, a transition from 4 µm/2.5 µm to 20 µm/10 µm (×5 area increase) decreases threshold standard deviation by 5.1 times. Therefore, there is an optimal value of components' area in terms of threshold deviation reduction.

The finite value of the threshold leads to wrong decisions when assessing the element values, in particular, elements, whose difference is equal to or less than threshold. To assess, how the threshold leads to calibration decline, a function-level simulation is used. In this type of simulation, an array of unit elements with random errors is generated. The number of generated arrays is 100. The generation of element values relies on assumption that error distribution is normal. To get dispersion of the element distribution, the mismatch of the current source is simulated by Monte-Carlo analysis. Statistics of the current source mismatch is shown in Fig. 7. The mean value is $40.35 \mu A$, the standard deviation of random errors is 0.23%, which converts into 2.1 mV at comparator inputs. The ratio of the threshold and standard deviation of the current source is 0.74, 0.15 and 0.14 relative to the threshold values in Table 1.

Table 1

Simulation results of the comparator threshold

For the simulation, the following sorting algorithms are considered: bubble sort, merge sort, quick sort and selection sort. For each algorithm, the maximum error between the results of an ideal sort and a certain sorting algorithm is calculated and averaged across all generated arrays. Then, the obtained error is normalized by the threshold values. In order to assess subsequent effect on the calibration results (i.e. INL), the 1F1D algorithm [6] is considered. This algorithm is the simplest one and is used for a demonstration of sorting accuracy effect on the calibration results. The maximum values of INL after calibration are normalized to the INL before calibration and then averaged over all 100 cases for a comprehensive assessment of the calibration effect. Since the threshold also covers negative values along with positive ones, both sign cases are considered.

Устройства и системы передачи, приема и обработки сигналов

Fig. 6. Threshold statistics

The results are presented in Tables 2 and 3 for different N resolutions and positive and negative threshold values respectively. In terms of positive threshold values, the best error and INL reduction is obtained by the selection sort. The bubble and merge sorts in some conditions demonstrate worse results than before calibration (normalized $INL > 1$).

Table 2

Simulation results of the calibration (positive threshold)

In terms of negative threshold values, the bubble sort has the best results, while the selection sort has the worst ones. Merge and selection sorts in some condition demonstrate worse results than before calibration. The results of merge and quick sorts weakly differ at both positive and negative thresholds, which makes them resilient to the threshold sign altering. However, in case of bubble and selection sorts the threshold sign matters and must be determined.

Conclusion

Mismatch and process variations between the comparator branches leads to an appearance of a comparator threshold. This threshold defines a difference between the input signals, when the comparator switches. If difference is smaller, the relation between the two elements cannot be reliably established

Fig. 7. Deviation of the current source value

Table 3

and the further calibration process may be unsuccessful. In particular, the finite threshold leads to wrong decisions during the sorting phase of switching-based calibration. This paper investigates the influence of comparator component mismatch on the results of switching-based calibration.

The simulation results of the comparator designed using 0.18 μ m "Mikron" HCMOS8D technology shows that there is an optimal comparator area in terms of threshold variation reduction. Increasing the components area is expected to reduce the standard deviation. Increasing of components by 5 times from 4 μ m/2.5 μ m to 20 μ m/10 μ m has corresponding reduction of the threshold standard deviation. However, further increasing the area cannot noticeably (3%) improve the comparison accuracy. Therefore, the component sizes of 20 μ m/10 μ m seem to be optimal values for the comparator.

The obtained comparison accuracy is verified by its influence on the results of the switching-based calibration. For this purpose, the 1F1D calibration algorithms are used as an example. In addition, the comparison accuracy has different effects on different sorting algorithms. The simulation of the calibration process shows that all sorting algorithms are able to establish almost correct order of the elements. However, for the smallest comparator variant $(4 \mu m/2.5 \mu m)$ only quick sort can provide INL improvement for all considered conditions. The medium comparator $(20 \mu m/10 \mu m)$ is able to provide a significant INL improvement (up to 61%). The largest comparator (100 μ m/50 μ m) has almost the same threshold and provides from 0.2% to 3% INL improvement compared to the medium comparator. Therefore, the largest comparator can be discarded as an impractical solution and the optimal comparator area can be used without significant losses.

As for the choice of the sorting algorithm, the quick sort is the most effective and reliable solution. Although bubble and selection sorts can show slightly better results, they are sensitive to the influence of the threshold sign.

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INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Yenuchenko Mikhail S. Енученко Михаил Сергеевич E-mail: mixeme@outlook.com ORCID: https://orcid.org/0000-0002-5301-3871 **Kvashina Natalya V. Квашина Наталья Владимировна** E-mail: kvashina.nv@gmail.com ORCID: https://orcid.org/0000-0003-2637-0846

Piatak Ivan M. Пятак Иван Михайлович E-mail: i.m.piatak@gmail.com

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