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MASH 2-2 DELTA-SIGMA MODULATOR WITH DYNAMIC ELEMENT MATCHING IN 0.18 µm CMOS TECHNOLOGY

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Abstract. Design details and results of post-layout simulation for multi-stage noise-shaping 2-2 delta-sigma modulator based on 0.18 µm CMOS from JSC Mikron are presented. The circuit consists of two similar 2nd order stages connected sequentially and based on fully differential operational transconductance amplifiers and switched capacitors. The delta-sigma modulator processes a differential input signal and has a two-bit quantizer, which is a simple 2-bit analog-to-digital converter that contains three differential comparators. A special digital circuit is used, which provides dynamic element matching, also known as dynamic weighted averaging in digital-to-analog converter, which is connected to the switched capacitors. Supply voltage is 1.8V. Clock frequency is 1 MHz. Frequency band of the input signal is up to 8 kHz. Dynamic range is 62 dB. Power consumption is 1.9 mW.

Keywords: ADC, DSM, switched capacitors, DEM, OTA, differential comparator, 2nd order

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ДЕЛЬТА-СИГМА-МОДУЛЯТОР СО СТРУКТУРОЙ MASH 2-2 И ДИНАМИЧЕСКИМ СОГЛАСОВАНИЕМ ЭЛЕМЕНТОВ ПО ТЕХНОЛОГИИ КМОП 0,18 МКМ

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Аннотация. Представлены процесс разработки и результаты моделирования в том числе с паразитными параметрами для многокаскадного дельта-сигма модулятора со структурой MASH 2-2 на основе технологии АО "Микрон" КМОП 0,18 мкм. Схема состоит из двух похожих каскадов 2-го порядка, соединённых последовательно и использующих полностью дифференциальные операционные транскондуктивные усилители и переключаемые конденсаторы. Дельта-сигма модулятор обрабатывает входной дифференциальный сигнал и имеет двухразрядный квантователь, который представляет собой простой 2-разрядный аналого-цифровой преобразователь, содержащий три дифференциальных компаратора. Применяется специальная цифровая схема, которая обеспечивает динамическое согласование элементов, также известное как динамическое взвешенное усреднение в цифро-аналоговом преобразователе, подключенном к массиву переключаемых конденсаторов. Напряжение питания составляет 1,8 В. Тактовая частота составляет 1 МГц. Диапазон частот входного сигнала составляет до 8 кГц. Динамический диапазон составляет 62 дБ. Потребляемая мощность составляет 1,9 мВт.

Ключевые слова: ДСМ, АЦП, переключаемые конденсаторы, ДСЭ, ОТУ, дифференциальный компаратор, второй порядок

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Introduction

Delta-sigma modulators achieve a high degree of insensitivity to analog circuit imperfections as they are based on a combination of oversampling and quantization error shaping techniques. This makes them the best choice in many cases for implementing on-chip analog-to-digital interfaces in today's integrated CMOS circuits. Increasing the analog-to-digital converter (ADC) resolution requires increasing the order of the delta-sigma modulator. Modulators up to the second order are stable circuits, to implement modulators of a higher order, Multi-stAge noise-SHaping (MASH) structures are used [1–6]. Another way to increase the ADC resolution is a multibit quantizer in the delta-sigma modulator which also demands a multibit digital-to-analog converter (DAC) in the feedback loop.

This paper presents realization of the MASH 2-2 delta-sigma modulator based on 0.18 μm CMOS from JSC Mikron. The paper is organized as follows. Section I gives a brief description of the delta-sigma modu-

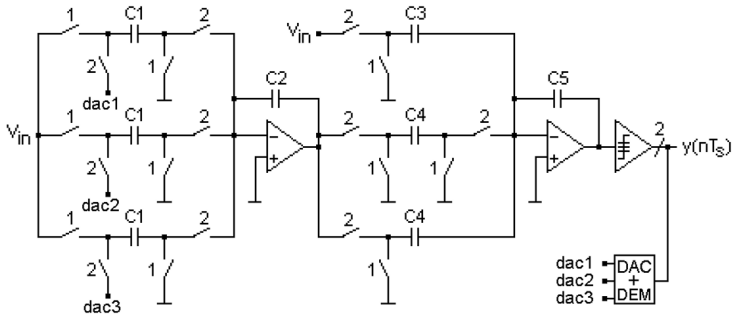

Fig. 1. Simplified structure of the unbalanced 2nd order delta-sigma modulator

lator structure based on switched capacitors. Section II presents the circuit for generating signals of phases to switch capacitors in the modulator. Section III describes the differential comparator for the ADC-DAC part, which is discussed in Section IV. Section V is devoted to the delta-sigma modulator layout and its simulation results. Finally, conclusions are given.

I. Delta-sigma modulator structure

The switched-capacitor delta-sigma modulator is designed in accordance with the recommendations of papers [7–10] as MASH 2-2. Its circuit consists of two similar 2nd order stages connected sequentially. A 2nd order stage is shown in Figure 1 as a simplified unbalanced circuit based on two operational transconductance amplifiers (OTAs). The quantizer is a simple 2-bit ADC that contains three differential comparators and generates the stage output code. The input signal of the delta-sigma modulator is supplied during the first phase to three switched capacitors in the first summing integrator, and during the second phase via direct connection to the second integrator. In the first integrator, during the second phase, the 2-bit signal of the digital-to-analog converter (DAC) is supplied to the switched capacitors. Here, DEM is dynamic element matching. The DAC output code is in unary form (digits are *dac*3, *dac*2, *dac*1). In the simplest case, the output signals of the comparators in thermometric code are supplied. In the second integrator, during the second phase, signals from one resistive element (based on a capacitor and four switches) and two capacitive elements are added. The capacitor ratios in Fig. 1 are given in the following proportions:
in both stages C1=0.5 pF and C2=3 pF, therefore, the attenuation coefficient in the first integrator is set to 3*C1/C2=1/2,
in the first stage C3=0.5 pF, C4=1 pF, and C5=2 pF, therefore, the attenuation coefficients in the second integrator of the first stage are set to C3/C4=1/2 and C4/C5=1/2,
in the second stage C3=0.5 pF, C4=1 pF, and C5=1 pF, therefore, the attenuation coefficients in the second integrator of the second stage are set to C3/C4=1/2 and C4/C5=1.

The integrators of the delta-sigma modulator are based on a fully differential OTA [10, 11]. The OTA core is the folded-cascode circuit, with the parallel connection of the p-type and n-type input differential pairs and has the differential rail-to-rail output. The OTA has 69.8 dB gain and unity gain bandwidth of 27.0 MHz and phase margin of 78.5 degrees at 5 pF load. The current consumption of OTA at the supply voltage of 1.8 V is about 200 μA. The amplifier noise referred to the input at 1 kHz is 383 nV/√Hz.

II. Circuit for generating signals of the first and second phases

The circuit for generating signals of the first and second phases is shown in Fig. 2, *a*. Based on the input clock signal *clk*, the circuit generates signals for the first and second phases, as well as the phase signals inverse to them. After passing through several inverters ‘inv’, the signal is fed to the delay line based on ‘inv’ and ‘inv_long’ (inverters with a large transistor length). Then, using NAND elements ‘nand’, the signals

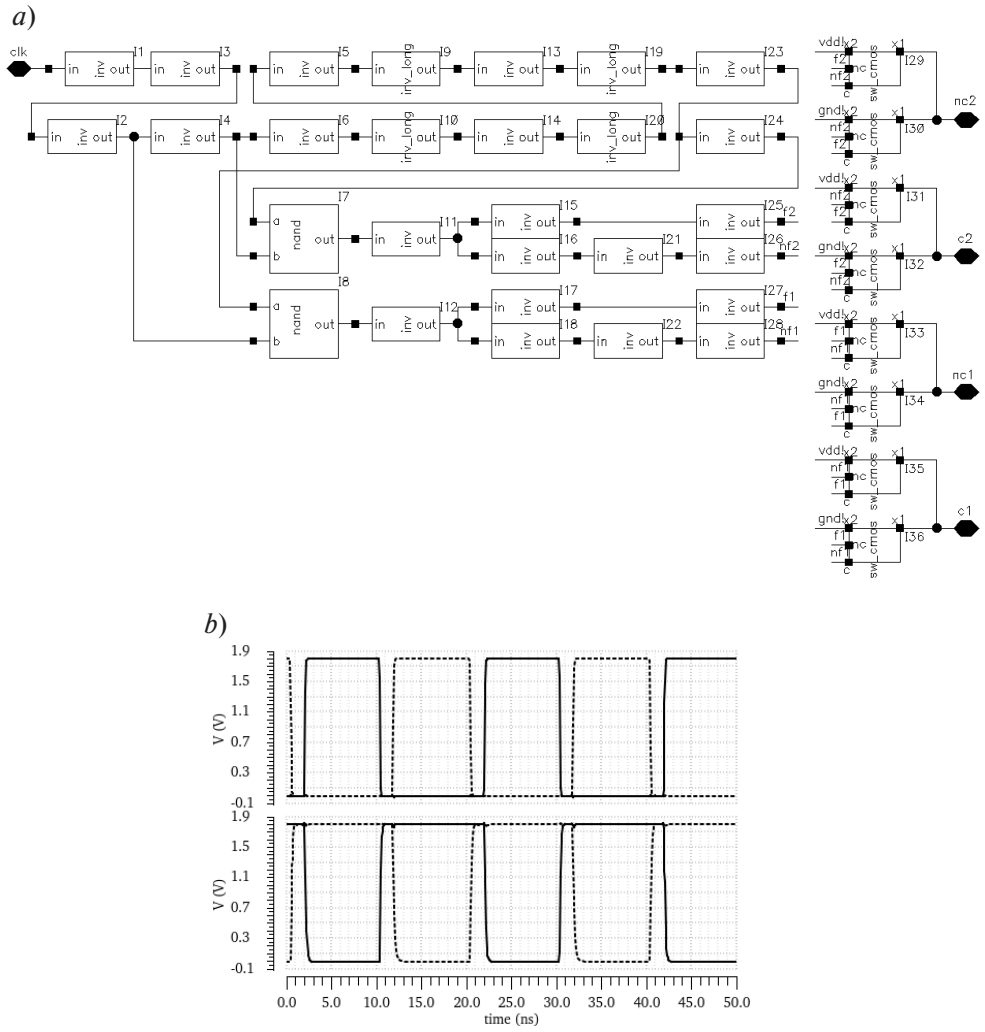

Fig. 2. Circuit for generating signals of the first and second phases (*a*); Simulation results (*b*)

before and after the delay line are multiplied, which makes it possible to create protective time intervals between the working phase intervals. In this way, signals *f*1, *nf*1, f2, *nf*2 are generated that control analog multiplexers based on CMOS switches 'sw_cmos'. The simulation results of the output signals *c*1, *nc*1 of the first phase and *c*2, *nc*2 of the second phase are shown in Fig. 2, *b* (*c*1 and *c*2 are on the top graph, *nc*1 and *nc*2 are on the bottom, with *c*2 and *nc*2 shown with the dotted line).

III. Differential comparator

The circuit of the differential comparator is shown in Fig. 3, *a*. The differential comparator has four inputs, two for the analog signals of the integrator *vp*, *vm* and two for the reference levels *vp*2, *vm*2. When the clock signal *clk* is at ground level, the input signals of the inverters 'inv' are equal to the supply voltage. When the clock signal *clk* becomes equal to the supply voltage, transistors M3, M6 go to cutoff, and the transistors M2, M10 make a decision depending on the comparison of currents through transistors M1 and M4, M7 and M11. Inverters 'inv' provide decoupling between the circuit core and the latch using NOR elements 'nor'. The latch stores the comparator decision while the core is in the reset phase, that is, when the clock signal *clk* is at ground. The simulation results of the differential comparator are shown in Fig. 3, *b*. The top graph shows the input signals. The analog signals of the integrator *vp*, *vm* are triangular, the reference levels *vp*2, *vm*2 are both equal to 900 mV, i.e. half the supply voltage.

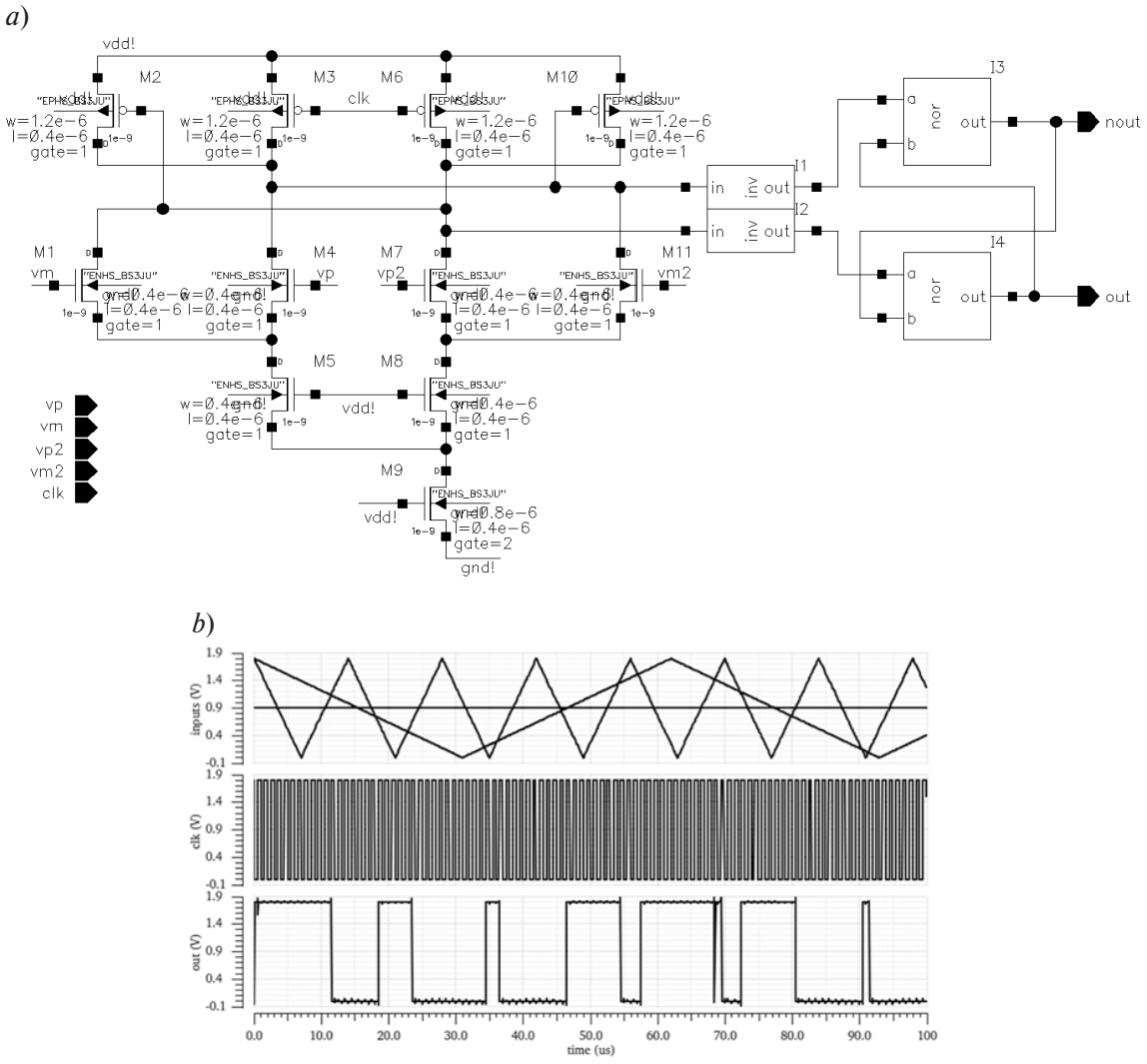

Fig. 3. Circuit of differential comparator (*a*); Simulation results (*b*)

IV. ADC-DAC part

The circuit of ADC-DAC part with DEM is shown in Fig. 4, *a*. The circuit contains a resistive divider, three comparators 'comparator' with output buffers on inverters 'inv', an adder 'adder' in accordance with paper [12, 13] as an encoder of the thermometric code *t*<1:3> into the binary code *b*<0:1> and analog multiplexers on CMOS switches 'sw_cmos' that generate DAC signals *th*<1:3> and *nth*<1:3>. In this circuit, the output signals of the DAC are not the same as the output signals of the comparators. A special digital circuit is used, consisting of D-flip-flops 'd_ff' and logic elements, which provides dynamic element matching (DEM), also known as dynamic weighted averaging [14, 15] in the DAC. The resistive divider is based on resistors with a nominal value of 11 kOhm. With the supply voltage of 1.8 V, the voltage levels in the *res*<1:3> nodes are 600 mV, 900 mV, 1200 mV, respectively.

Due to the variation in the values of the elements, the transfer curve of the DAC turns out to be non-linear. The nonlinearity of the DAC leads to the appearance of unwanted harmonics in the operating frequency range of the modulator spectrum. In Fig. 1, a unary DAC is used consisting of three capacitors of the same value, let's denote them A, B, C. As can be seen from Table 1, depending on the 2-bit output code of the modulator, no element of the DAC is connected or 1, 2 or 3 elements are connected. Table 1 shows three options for connecting the elements. If only one of them is used, the effect of mismatch on

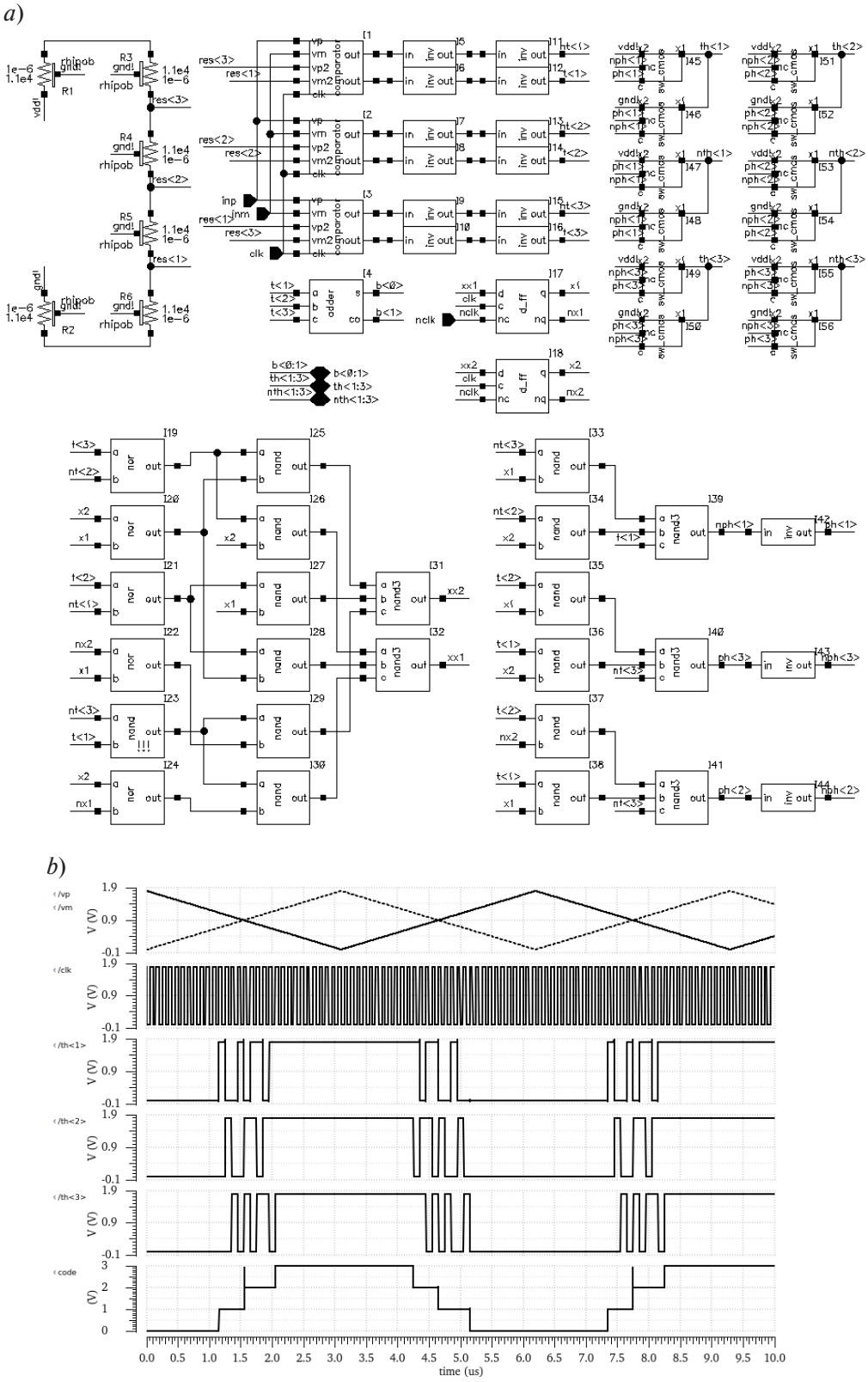

Fig. 4. Circuit of ADC-DAC part with DEM (*a*); Simulation results (*b*)

the nonlinearity of the DAC is maximally negative. If the connection options are used alternately, then the nonlinearity of the DAC is averaged and reduced by √3 times. If the cyclical appearance of options for connecting the elements is excluded, the nonlinearity will turn into noise.

Table 1

Operating principle DEM of the DAC control circuit

b<1:0>	t<3:1>	Options for connecting the elements		
		x2x1		
		00	01	10
00	000	–	–	–
01	001	A	B	C
10	011	A + B	B + C	C + A
11	111	A + B + C	B + C + A	C + A + B

The simplest way to use options for connecting the elements is one after another. However, the connection option is only important in two cases of the input code 01 and 10, when one or two elements are connected. Therefore, it is advisable to switch to the next option only in these two cases. In addition, it is possible to switch options clockwise when code 01 appears and counterclockwise when code 10 appears. Since these codes have an equal probability of occurrence, switching will occur at random times in a random direction. For this case, the logical expressions in the circuit (see bottom of Fig. 4 *a*) have the following form

$$xx2 = \overline{\overline{t3 + \overline{t2}} \cdot \overline{x2 + x1} \cdot \overline{t2 + \overline{t1} \cdot x1} \cdot \overline{\overline{t3} \cdot t1} \cdot \overline{x2 + x1}};$$

$$xx1 = \overline{\overline{t3 + \overline{t2}} \cdot x2 \cdot \overline{t2 + \overline{t1} \cdot \overline{x2 + x1}} \cdot \overline{\overline{t3} \cdot t1} \cdot \overline{x2 + x1}};$$

$$ph3 = \overline{\overline{t2 \cdot x1} \cdot \overline{t1 \cdot x2} \cdot \overline{t3}};$$

$$ph2 = \overline{\overline{t2 \cdot \overline{x2}} \cdot \overline{t1 \cdot x1} \cdot \overline{t3}};$$

$$\overline{ph1} = \overline{\overline{t3} \cdot x1 \cdot \overline{t2} \cdot x2 \cdot t1}.$$

As depicted in Fig. 4, *a*, signals *xx*2 and *xx*1 act on the inputs of D flip-flops ‘d_ff’ and are stored for one clock cycle of *clk*, and signals *ph*<1:3> and *nph*<1:3> control multiplexers based on CMOS switches ‘sw_cmos’ that form DAC output signals *th*<1:3> and *nth*<1:3>.

The simulation results of ADC-DAC part with DEM is shown in Fig. 4, *b*. The input signals *vp*, *vm*, clock signal *clk*, DAC signals *th*<1:3> and the code signal *code*=2**b*<1>+*b*<0> formed from the output bits are presented. As seen, when *code* is equal to 1 or 2, the signals to control DAC *th*<1:3> are switched according to the described idea, which leads to error averaging and compensates for the nonlinearity of the DAC transfer curve.

V. Delta-sigma modulator layout and simulation results

The delta-sigma modulator layout is shown in Fig. 5. Sizes of the layout are 430 μm × 220 μm. The circuit consists of two similar stages connected sequentially. The attenuation coefficients in the second integrator of the first and second stages are different, so capacitor arrays look different. The last OTA in the second stage has half the load in comparison with other OTAs. Thus sizes of the last OTA layout are 32 μm × 35 μm, while sizes of other OTAs are 51 μm × 35 μm. The last OTA has 68.7 dB gain, and at 2.5 pF load it shows a unity gain bandwidth of 27.5 MHz and phase margin of 78.4 degrees. The current consumption of the last OTA at the supply voltage of 1.8 V is about 120 μA. The last amplifier noise referred to the input at 1 kHz is 450 nV/√Hz.

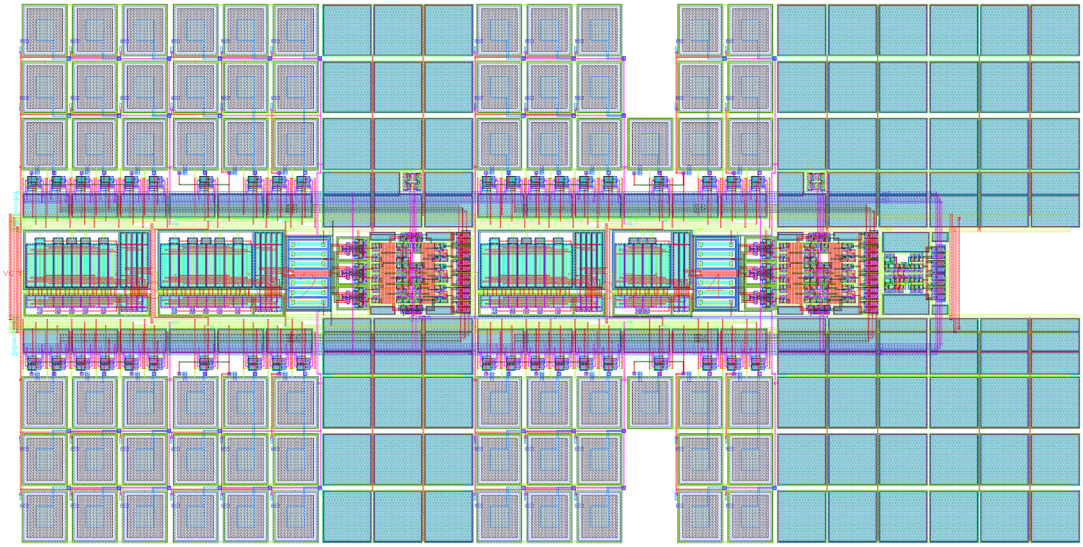

Fig. 5. Delta-sigma modulator layout

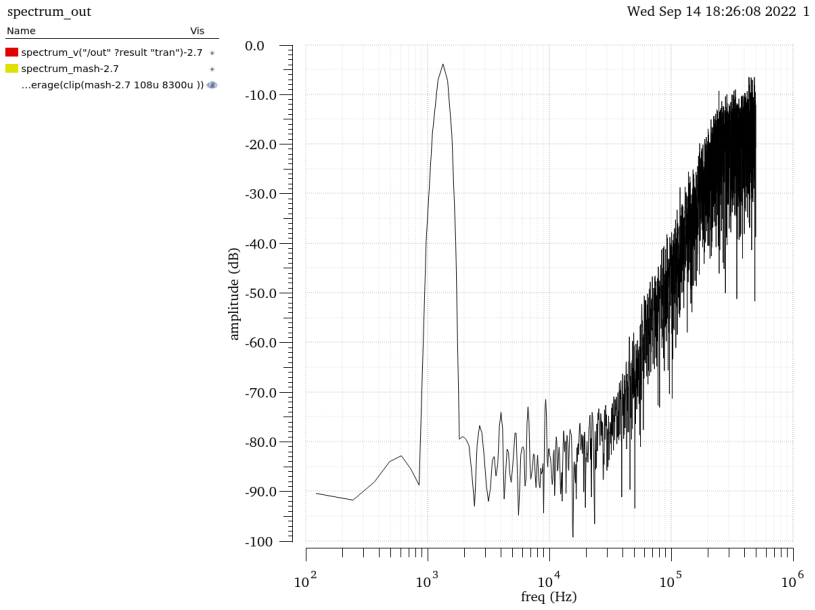

Fig. 6. Simulation results of delta-sigma modulator

Post-layout simulation results of the delta-sigma modulator are shown in Fig. 6. The output code was composed from two 2-bit outputs of the first and second stages. From the spectrum, the 4th order noise shaping property can be seen. At the clock frequency of 1 MHz and the frequency band of the input signal up to 8 kHz, the dynamic range is 62 dB. Power consumption is 1.9 mW.

Conclusions

Realization of the MASH 2-2 delta-sigma modulator based on 0.18 μm CMOS technology from JSC Mikron is described. Supply voltage is 1.8 V. Clock frequency is 1 MHz. Frequency band of the input signal is up to 8 kHz. The delta-sigma modulator layout occupies an area of 430 μm × 220 μm. Post-layout simulation results of the delta-sigma modulator are given. Dynamic range is 62 dB. Power consumption is 1.9 mW.

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