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A LOW-POWER DIGITALLY CONTROLLED OSCILLATOR BASED ON 65-nm CMOS TECHNOLOGY

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This paper contains the research results related to the Master thesis about the design of Dual band Differential Digital Ring oscillator (DRO) in two stages, describing the lower power consumption, smaller area, lower phase noise, linear frequency range and better frequency stability with variation of applied voltage, in addition to the investigation of the temperature variation effect. We have proposed a circuit using the 65-nm CMOS process with Radio Frequency (RF) transistors and the output frequency digitally controlled (by 4-bit (coarse), 3-bit (fine) tuning) as control code, for the low-band frequency range [1.487–3.021 GHz] and power consumption of 0.359 mW @ 2.42 GHz, and for the high-band frequency range [3.5–6.98 GHz] and the power consumption of 1.86 mW @ 6.023 GHz, the band gap between two bands equal to 500 MHz, the phase noise about −84.4 dBc/Hz @ 1MHz, and the jitter value of 4.335 ps, with FOM equal to −156.5 dBc/Hz.

Keywords: 65-nm technology; DCO; positive feedback, power consumption; buffer; cadence software.

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ГЕНЕРАТОР, УПРАВЛЯМЫЙ ЦИФРОВЫМ КОДОМ, С ПОНИЖЕННЫМ ЭНЕРГОПОТРЕБЛЕНИЕМ НА ОСНОВЕ 65 нм КМОП-ТЕХНОЛОГИИ

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Изложены результаты исследований, связанных с магистерской диссертацией о конструкции двухканального дифференциального генератора цифровых колец (DRO) в два этапа, что отвечает за большую часть потребления энергии, меньшую площадь, более низкий фазовый шум, линейный частотный диапазон и лучшую стабильность частоты с изменением приложенного напряжения в дополнение к исследованию эффекта изменения температуры. Предложена схема двухдиапазонного генератора, разработанного с использованием параметров КМОП-технологии с разрешением 65 нм. Выходная частота генератора управляется в диапазонах 1,49–3,02 ГГц и 3,50–6,90 ГГц 4-разрядным цифровым кодом для грубой настройки и 3-разрядным – для точной настройки. Потребляемая мощность составляет 0,36 мВт и 1,86 мВт соответственно в каж-

дом диапазоне; уровень фазовых шумов – не более минус 84,4 дБс/Гц при отстройке 1 МГц; значение джиттера – не более 4,3 пс; комплексный параметр качества (FOM) – минус 156,5 дБс/Гц.

Ключевые слова: 65-нм технология; ИДК; положительная обратная связь; энергопотребление; буфер; программное обеспечение cadence.

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The wireless systems are closely linked to the phenomenal success of the CMOS technology scaling that makes it possible to develop increasingly complicated systems on a single silicon chip while preserving performance and functionality at an ever lower cost, lower power consumption, smaller product size and an increaded unity gain of CMOS transistors [1, 2]. Concerning wireless systems, LC circuits in controlled voltage oscillators and large-sized capacitors in filters used in frequency synthesizers are less suitable for scalability. In contrast, all-digital phase-locked loops (ADPLL) based on digitally controlled oscillators (DCO) can be easily integrated into the digital system and have much less dependence on temperature, process and voltage variations. The ADPLL architecture still entails significant levels of power consumption and silicon area in a nanoscale CMOS, which allows for further power and cost reductions. The focus is on analyzing and tracking the advances in the DCO base depending on its performance level. As we knew that the digitally controlled oscillator has many types and topologies and because the Differential Ring Digital- Controlled-Oscillator (DRO) is better in frequency stability with power supply voltage variations and has lower phase noise, a DRO using the 65-nm technology in a two delay stages is proposed.

In this paper, the differential Digital-Controlled-Oscillator (DCO) with a reconfigurable delay cell in each two stages of a digitally controlled ring oscillator is proposed. The DCO operates in two bands: 1.40–3.02 GHz and 3.50–6.98 GHz in comparison with the architecture proposed in [3]. Each band has 128

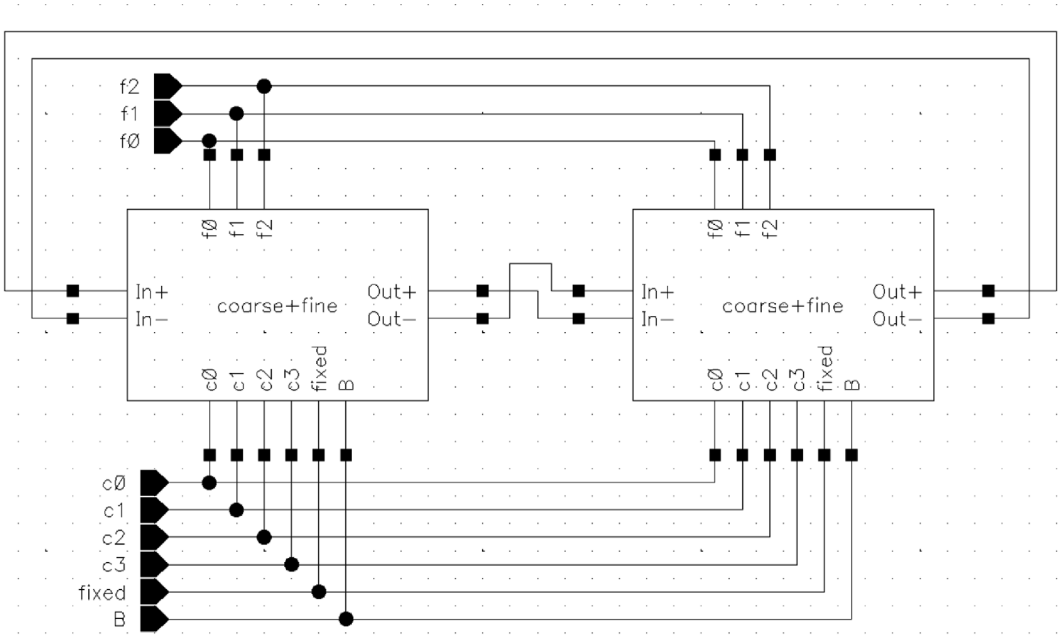

Fig. 1. DCO structure

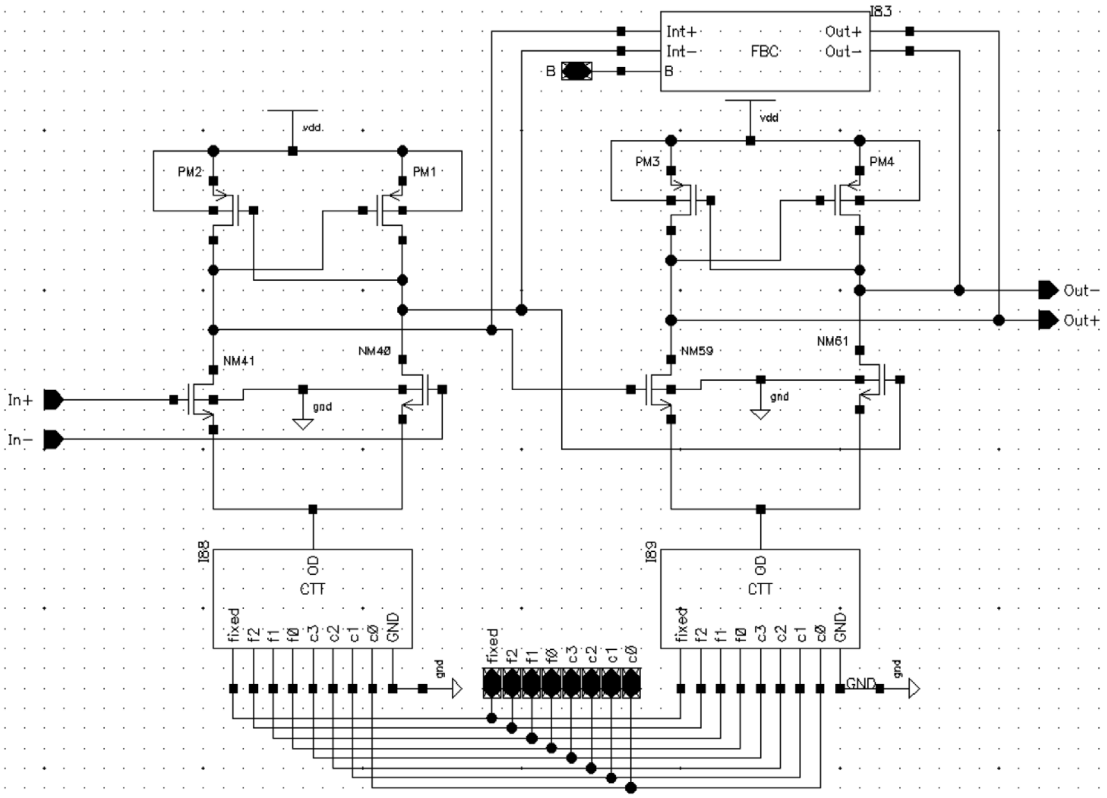

Fig. 2. Schematic of the delay element

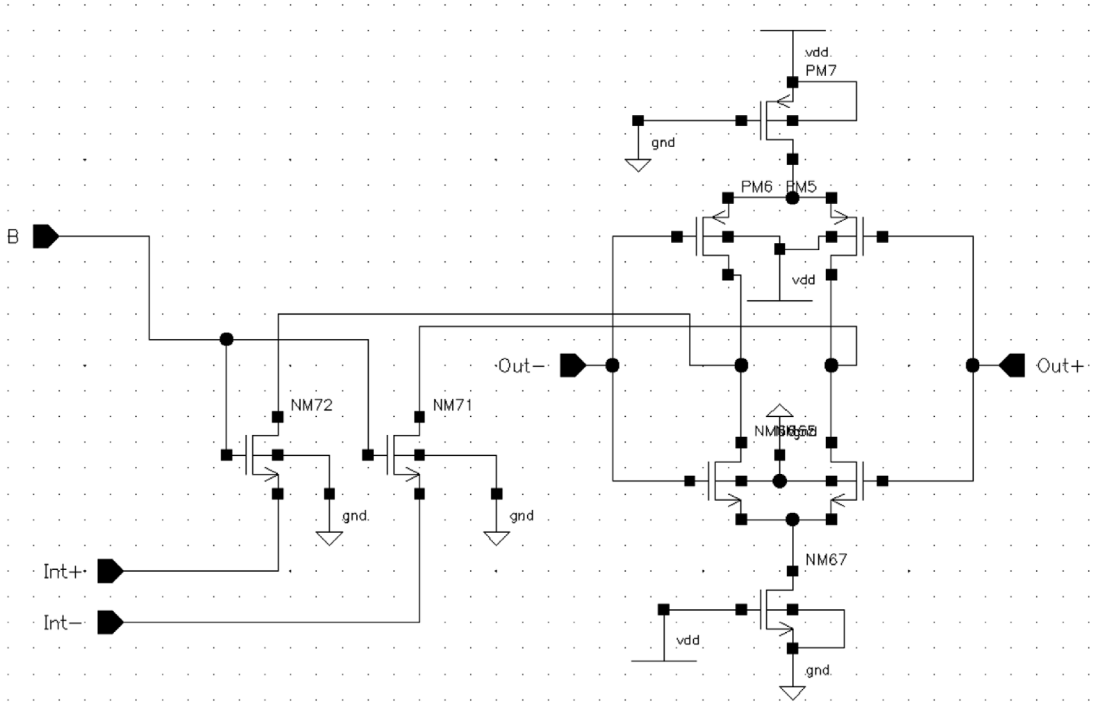

Fig. 3. Schematic of the «FBC»

sub-bands controlled by the 7-bit digital word, a new SCL-based delay cell is used which has a reconfigurable structure. Fig. 1 shows the proposed dual band DCO with a block diagram of delay elements.

Each delay element has the following pins: pin «B» defines the current band, pins «C0» – «C3» «F0», «F1», «F2» define the upper and lower bits of the digital control word. The schematic of the delay element is shown in Fig. 2

Contrary to the traditional trigger structure, a new feedback circuit «FBC» is included into the scheme. When the signal on pin «B» is low, total propagation delay increases and the circuit operates at a lower frequency band. When the signal on pin «B» is kept high, the propagation delay decreases and frequency of oscillation rises. Block «CTT» contains a bank of transistors which are used to set the tail current of the differential pair. Schematic of the «FBC» is shown in Fig. 3.

Introducing a positive feedback into the trigger scheme allows using the same control signals for frequency control within each band. The frequency variations depending on the control word for low and high band are shown in Fig. 4 and Fig. 5, respectively.

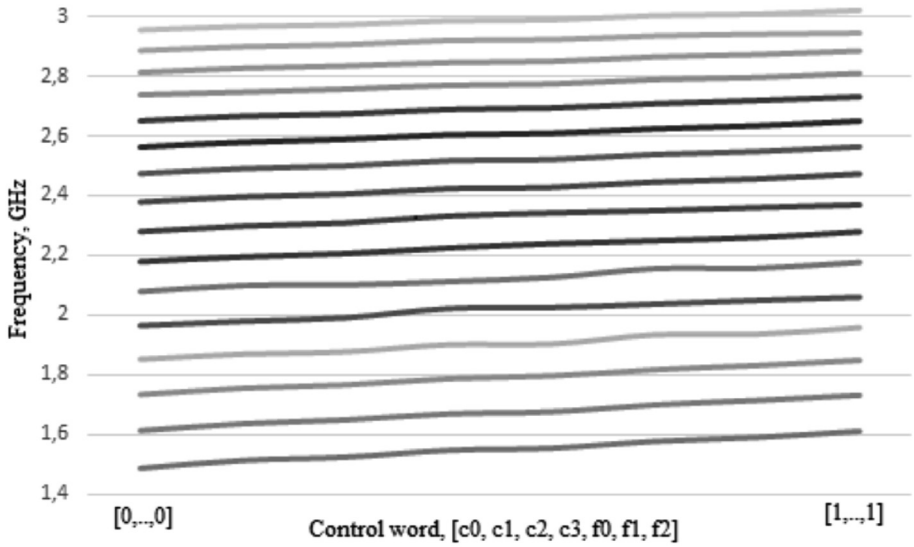

Fig. 4. Frequency of oscillation vs digital control word (Low band)

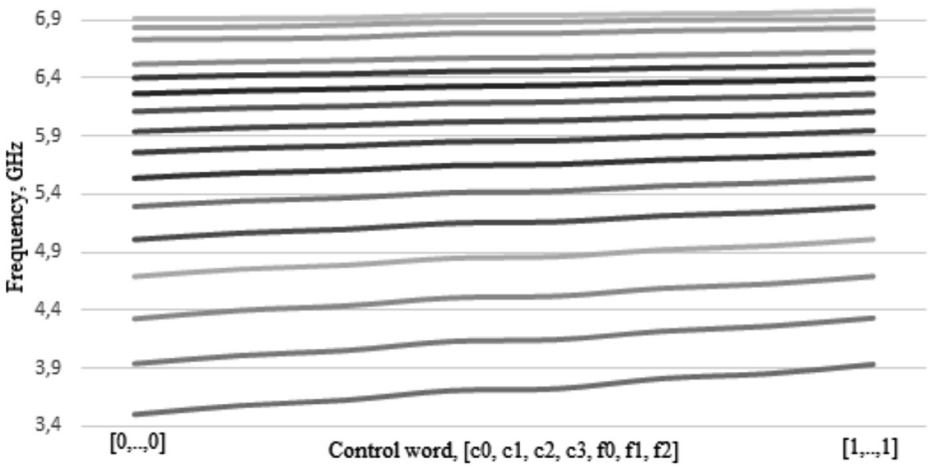

Fig. 5. Frequency of oscillation vs digital control word (High band)

Comparison of this study with the 65-nm technology

Ref.	Tech (nm)	Vdd (V)	Bit word	Frequency range	Power consumption	Phase noise (dBc/Hz)	Jitter (ps)	FOM (dBc/Hz)	Topology
This work	65	1	7 +1	Low band 1.48–3.02 GHz	0.359 mW @ 2.42 GHz	−84.4 @ 1 MHz	4.335	−156.5	Dual band DRO
				High band 3.5–6.98 GHz	1.86 mW @ 6.023 GHz				
[5]	65	1	5	47.8–538.7 MHz	0.142–0.205 mW	-	13.2 @ 64.4 MHz	-	Cascading cell base
[6]	65	1.8	14	5 GHz	2.16 mW	−149.1 @ 10 kHz	0.42	-	DRO
[7]	65	1.2	-	4.1–6.5 GHz	18 mW	−145 @ 1 MHz	-	−186.6	QDCO
[8]	65	1.2	4	1.67–2.45 GHz	7 mW	−78 @ 1 MHz	-	-	L based DCO
[9]	65	1	14	5.01 GHz	3.7 mW	−150 to −107 @ 1 MHz	0.45	−247.4	LC DCO
[10]	65	0.45	2	3.2 MHz	90 nW	−95 @ 1 MHz.	6.39	−150.6	DCLO
[11]	65	0.5	-	43.5–152 MHz	59 μW	−103.4 @ 1 MHz	-	−155.7	Relaxation DCO

The low band and high band cover approximately 1.5 and 3.4 GHz frequency range respectively. The covered frequency range is enough to compensate the influence of the technological process and the temperature on the DCO tuning range.

The comparison of the proposed dual band DCO with the other study is summarized in Table.

Conclusion

The proposed DCO is designed in the 65-nm UMC CMOS technology. It achieves 0.35 mW and 1.86 mW power consumption at 2.4 and 5 GHz bands respectively. The expected jitter for both bands is not more than 4.33 ps and FOM is equal to 156.5 dBc/Hz. The phase noise is less than −84.4 dBc/Hz for both bands.

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